C4H22W500A

Power GaN transistor

Rev. 1 — 24 September 2021

AMPLEON

Product data sheet

1. Product profile

1.1 General description

500 W GaN packaged asymmetric Doherty power transistor for base station applications at frequencies from 2110 MHz to 2170 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty application demo circuit. V_{DS} = 50 V; I_{Dq} = 450 mA (main), $V_{GS(amp)peak}$ = −6.0 V, unless otherwise specified.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR	$P_{L(5dB)}$
	(MHz)	(mA)	(V)	(dBm)	(dB)	(%)	(dBc)	(dBm)
1-carrier W-CDMA [1]	2110 to 2170	450	50	49.2	16.3	59.8	−31.2	-
pulsed CW [2]	2110 to 2170	450	50	-	-	-	-	56.9

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 10.5 dB at 0.01 % probability on CCDF.

[2] Test signal: pulsed CW; t_p = 30 μs; δ = 35 %.

1.2 Features and benefits

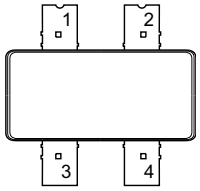
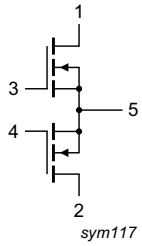
- Excellent digital pre-distortion capability
- High efficiency
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Internally matched for ease of use

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 2110 MHz to 2170 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1273-1	C4H22W500AZ	9349 604 84517	Tray; 20-fold; dry pack	60
	C4H22W500AY	9349 604 84518	TR13; 100-fold; 44 mm; dry pack	100

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	operating	-	52	V
V_{DS}	drain-source voltage	V_{GS} = −8 V	-	150	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		−15	+2	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		−15	+2	V
$I_{GF(amp)main}$	main amplifier forward gate current		-	31.2	mA
$I_{GF(amp)peak}$	peak amplifier forward gate current		-	37.8	mA
T_{stg}	storage temperature		−65	+150	°C
T_{ch}	active die channel temperature	[1]	-	275	°C
T_{case}	case temperature	operating [1]	−40	+130	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(s\text{-}c)(IR)}$ [1][3]	thermal resistance from active die surface to case by Infrared measurement	V_{DS} = 48 V; I_{Dq} = 620 mA; $V_{GS(amp)peak}$ = −6.5 V; T_{case} = 80 °C; CW; P_L = 80 W; P_{dis} = 87 W	0.62	K/W
$R_{th(ch\text{-}c)(FEA)}$ [2][3][4]	thermal resistance from active die channel to case by Finite Element Analysis	T_{case} = 80 °C; P_{dis} = 92 W	0.92	K/W

[1] Infrared (IR) thermal values are for reference only and cannot be used to determine performance or reliability.

[2] Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

[3] P_{dis} is total Doherty dissipation power which includes main and peak amplifier.

[4] Peak amplifier is assumed to contribute 10 % Doherty dissipation power.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 31.2 mA	−3.25	−2.72	−1.95	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 624 mA	−3.25	−2.60	−1.95	V
$I_{D(leak)}$	drain leakage current	V_{GS} = −10 V; V_{DS} = 50 V	-	-	7.55	mA
I_{GSS}	gate leakage current	V_{GS} = −8 V; V_{DS} = 0 V	-	-	1.51	mA
Peak device						
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 37.8 mA	−3.25	−2.67	−1.95	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 756 mA	−3.25	−2.60	−1.95	V
$I_{D(leak)}$	drain leakage current	V_{GS} = −10 V; V_{DS} = 50 V	-	-	9.15	mA
I_{GSS}	gate leakage current	V_{GS} = −8 V; V_{DS} = 0 V	-	-	1.83	mA

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2167.5 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; $V_{GS(amp)peak}$ = −5.7 V (typical); T_{case} = 25 °C; unless otherwise specified; in a Doherty production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 83.2 W	15.0	16.0	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 83.2 W	49.0	54.0	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 83.2 W	-	−9	−6	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 83.2 W	-	−27.0	−24.0	dBc

Table 8. RF characteristics

Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; f = 2170 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; $V_{GS(amp)peak}$ = −5.7 V (typical); T_{case} = 25 °C; unless otherwise specified; in a Doherty production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	-	380	450	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The C4H22W500A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 48 V; I_{Dq} = 620 mA; $V_{GS(amp)peak}$ = −6.0 V; P_L = 440 W (pulsed CW; t_p = 100 μs; δ = 10 %); f = 2110 MHz; tested on the Doherty development RF test circuit.

7.2 Impedance information

Table 9. Typical impedance of maximum power and drain efficiency

Measured load-pull data (main device); all data measured on a harmonic impedance non-optimized load-pull fixture; I_{Dq} = 620 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 μs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)
Maximum power load						
2110	6.9 – j12.0	2.7 – j2.7	54.3	269	64.2	15.2
2140	7.6 – j12.3	2.7 – j2.7	54.4	275	65.4	15.1
2170	9.1 – j13.3	2.5 – j3.0	54.4	275	64.8	15.3
Maximum drain efficiency load						
2110	6.9 – j12.0	2.0 – j0.7	53.2	209	78.6	16.6
2140	7.6 – j12.3	1.3 – j0.6	51.9	155	77.2	16.6
2170	9.1 – j13.3	2.0 – j0.7	52.9	195	79.9	17.3

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of maximum power and drain efficiency

Measured load-pull data (peak device); all data measured on a harmonic impedance non-optimized load-pull fixture; I_{Dq} = 720 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 μs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)
Maximum power load						
2110	5.5 – j11.1	2.5 – j3.0	55.7	372	63.2	14.9
2140	6.1 – j11.4	2.7 – j2.7	55.6	363	67.4	15.1
2170	6.9 – j12.4	2.5 – j3.0	55.5	355	63.1	15.4
Maximum drain efficiency load						
2110	5.5 – j11.1	2.0 – j0.7	53.9	245	76.6	16.8
2140	6.1 – j11.4	1.3 – j0.6	52.7	186	74.7	16.5
2170	6.9 – j12.4	2.0 – j1.0	53.8	240	73.6	17.2

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

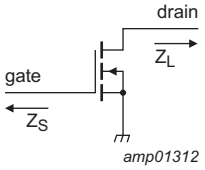
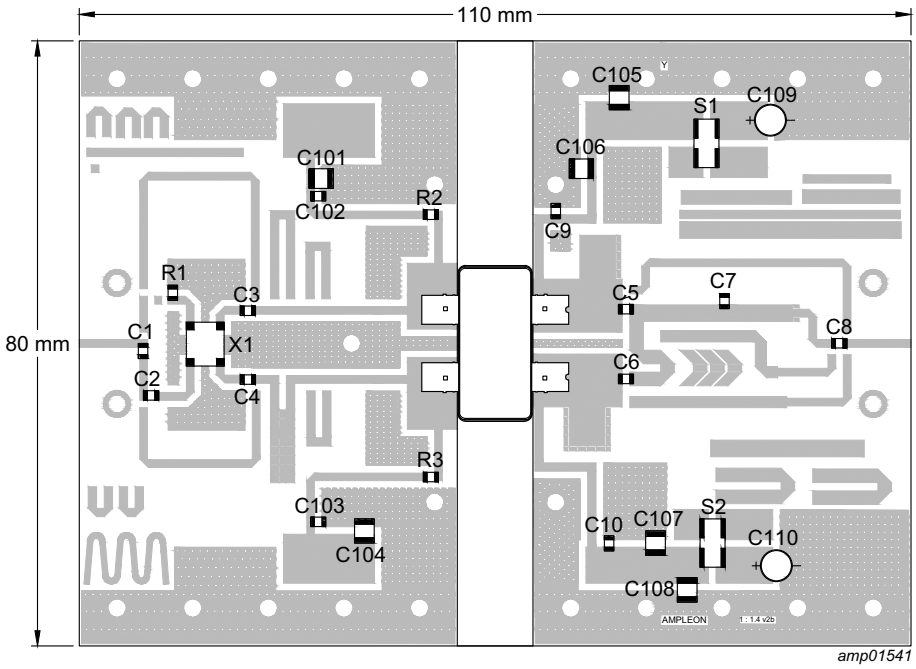


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.66; thickness = 0.508 mm; thickness copper plating = 35 μm.
See Table 11 for a list of components.

Fig 2. Component layout for test circuit

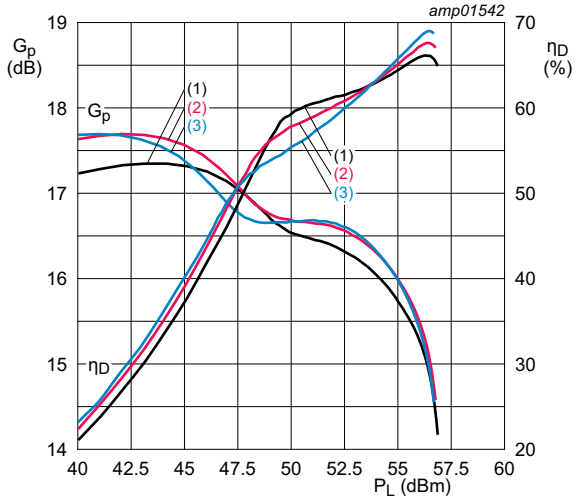
Table 11. List of components
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C8, C9, C10, C102, C103	multilayer ceramic chip capacitor	10 pF	ATC 600F
C5	multilayer ceramic chip capacitor	2.2 pF	ATC 600F
C6	multilayer ceramic chip capacitor	3.0 pF	ATC 600F
C7	multilayer ceramic chip capacitor	0.3 pF	ATC 600F
C101, C104, C105, C106, C107, C108	multilayer ceramic chip capacitor	10 μF, 100 V	Murata: SMD 1210
C109, C110	electrolytic capacitor	1000 μF, 100 V	
X1	hybrid coupler		Anaren: CMX21Q03
R1	resistor	51 Ω	SMD 1206
R2, R3	resistor	5.6 Ω	SMD 0805
S1, S2	current sense resistor	10 mΩ	LVK25 (1224)

7.4 Graphical data

All data are measured on the Doherty development RF test circuit.

7.4.1 Pulsed CW



V_{DS} = 48 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = −5.3 V; t_p = 100 µs; δ = 10 %.

(1) f = 2110 MHz

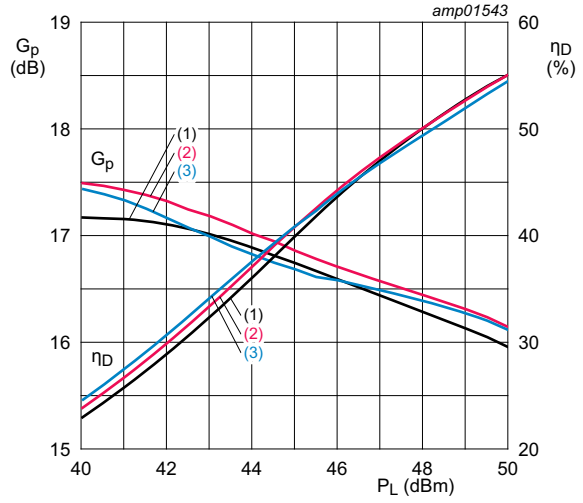
(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH.



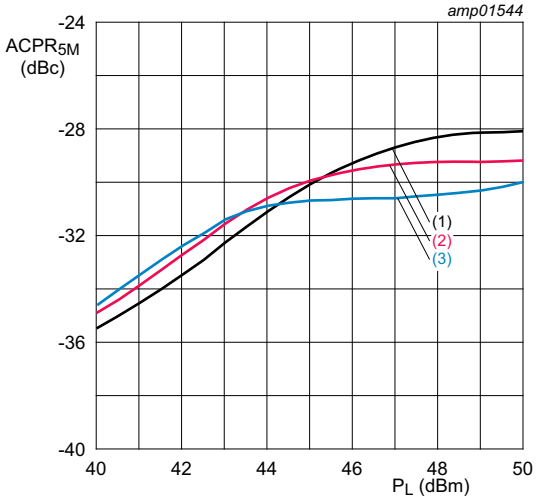
V_{DS} = 48 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = –5.3 V.

(1) f = 2112.5 MHz

(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 4. Power gain and drain efficiency as function of average output power; typical values



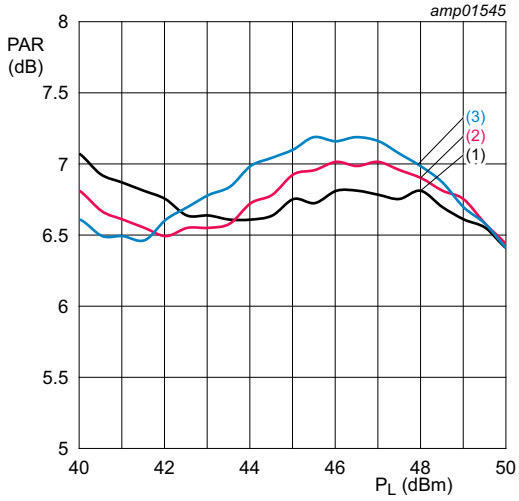
V_{DS} = 48 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = –5.3 V.

(1) f = 2112.5 MHz

(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = –5.3 V.

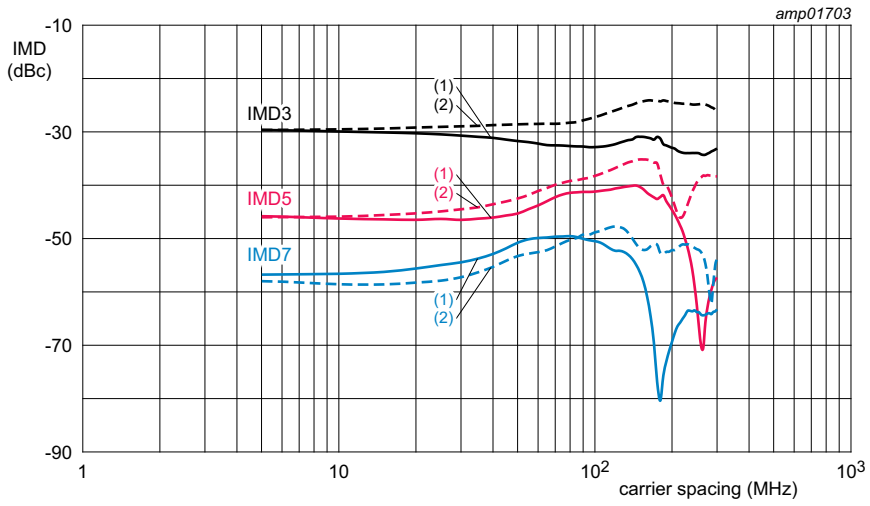
(1) f = 2112.5 MHz

(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Tone VBW



V_{DS} = 50 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = −5 V; f_c = 2140 MHz; P_L = 41 dBm; test signal: CW.

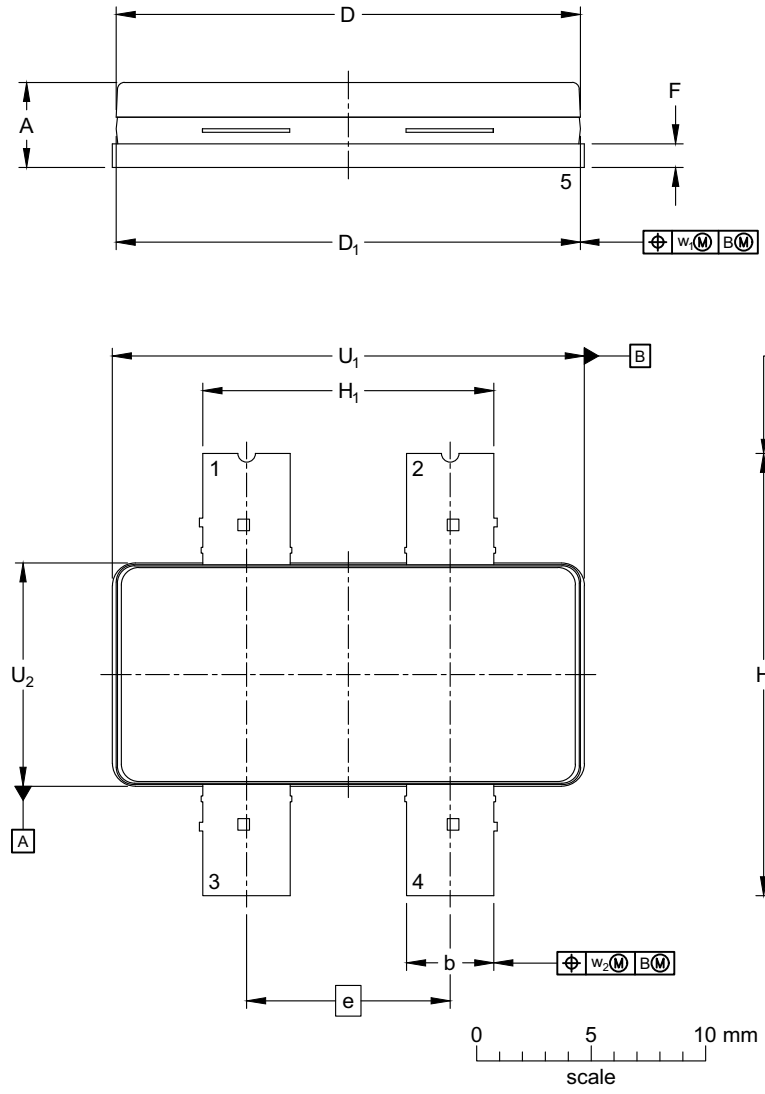
(1) IMD low

(2) IMD high

Fig 7. VBW capability

8. Package outline

Air cavity plastic earless flanged package; 4 leads SOT1273-1



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Note:
1. Dimension Q is measured at 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1273-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1273-1						17-01-12

Fig 8. Package outline SOT1273-1

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1B [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 1B is granted to any part that passes after exposure to an ESD pulse of 500 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
GaN	Gallium Nitride
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
C4H22W500A v.1	20210924	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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