Low I_Q Boost/SEPIC/Inverting Converter with 3A, 40V Switch

FEATURES

- **Wide Input Voltage Range: 2.8V to 40V**
- **Ultralow Quiescent Current and Low Ripple**
- **Burst Mode® Operation: I_Q = 9µA**
- **3A, 40V Power Switch**
- **Positive or Negative Output Voltage Programming with a Single Feedback Pin**
- **Programmable Frequency (300kHz to 2MHz)**
- Synchronizable to an External Clock
- Spread Spectrum Frequency Modulation for Low EMI
- Bias Pin for Higher Efficiency
- Programmable Undervoltage Lockout (UVLO)
- Overcurrent and Overtemperature Protection
- Thermally Enhanced 10-Lead 3mm × 3mm DFN Package

APPLICATIONS

- Industrial and Automotive
- Telecom
- Medical Diagnostic Equipment
- Portable Electronics

DESCRIPTION

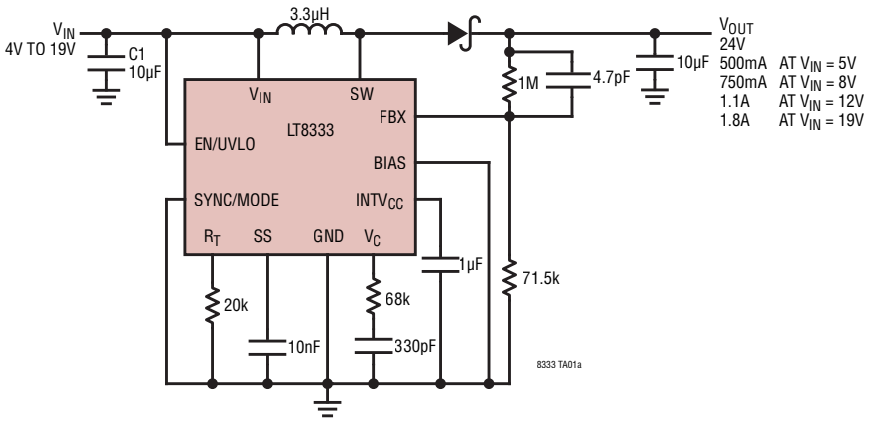
The LT®8333 is a current mode DC/DC converter with a 40V, 3A switch operating from a 2.8V to 40V input. With a unique single feedback pin architecture, it is capable of boost, SEPIC or inverting configurations. Burst Mode operation consumes as low as 9µA quiescent current to maintain high efficiency at very low output currents, while keeping typical output ripple below 15mV.

An external compensation pin allows optimization of loop bandwidth over a wide range of input and output voltages and programmable switching frequencies between 300kHz and 2MHz. A SYNC/MODE pin allows synchronization to an external clock. It can also be used to select between BURST or PULSE SKIP modes of operation with spread spectrum frequency modulation for low EMI. For increased efficiency, a BIAS pin can accept a second input to supply the $INTV_{CC}$ regulator. Additional features include frequency foldback and programmable soft-start to control inductor current during start-up.

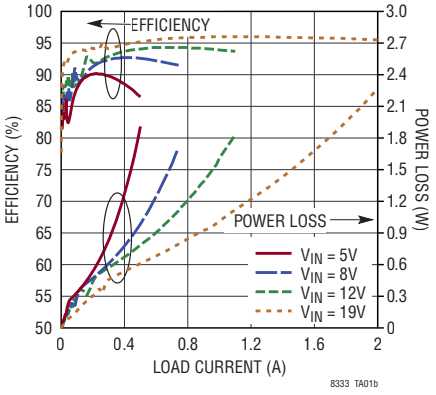
The LT8333 is available in a thermally enhanced 10-lead 3mm × 3mm DFN package.

TYPICAL APPLICATION

2MHz, 4V to 19V Input, 24V Output Boost Converter



Efficiency and Power Loss

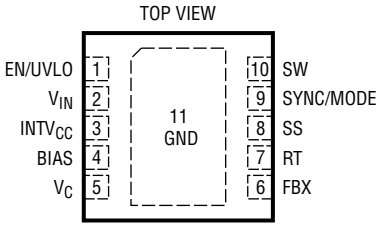


ABSOLUTE MAXIMUM RATINGS

(Note 1)

SW 40V
V_{IN}, EN/UVLO 40V
BIAS 40V
SYNC 6V
$INTV_{CC}$ ..... (Note 2)
VC 4V
FBX ..... ±4V
Operating Junction Temperature Range (Notes 3)
LT8333R ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Junction Temperature ..... +150°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS PGND AND GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8333RDD#PBF	LT8333RDD#TRPBF	LHQJ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, EN/UVLO = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range		●	2.8		40	V
V_{IN} Quiescent Current at Shutdown	$V_{EN/UVLO}$ = 0.2V	 ●		1 1	2 15	µA µA
	$V_{EN/UVLO}$ = 1.5V	 ●		2 2	5 25	µA µA
V_{IN} Quiescent Current						
Sleep Mode (Not Switching)	SYNC = 0V	 ●		9 9	15 30	µA µA
Active Mode (Not Switching)	SYNC = 0V or $INTV_{CC}$, BIAS = 0V	 ●		1200 1200	1600 1850	µA µA
	SYNC = 0V or $INTV_{CC}$, BIAS = 5V	 ●		22 22	40 65	µA µA
BIAS Threshold	Rising, BIAS Can Supply $INTV_{CC}$ Falling, BIAS Cannot Supply $INTV_{CC}$			4.4 4	4.65 4.25	V V
V_{IN} Falling Threshold to Supply $INTV_{CC}$	BIAS = 12V			BIAS – 2V		V
BIAS Falling Threshold to Supply $INTV_{CC}$	V_{IN} = 12V			V_{IN}		V
FBX Regulation						
FBX Regulation Voltage	FBX > 0V FBX < 0V	● ●	1.568 –0.822	1.6 –0.80	1.636 –0.780	V V
FBX Line Regulation	FBX > 0V, 2.8V < V_{IN} < 40V FBX < 0V, 2.8V < V_{IN} < 40V			0.005 0.005	0.015 0.015	%/V %/V
FBX Pin Current	FBX = 1.6V, –0.8V	●	–10		10	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, EN/UVLO = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator						
Switching Frequency (f_{OSC})	R_T = 165k R_T = 45.3k R_T = 20k	● ● ●	265 0.90 1.85	300 1 2	327 1.08 2.15	kHz MHz MHz
SSFM Maximum Frequency Deviation	(Δ_f/f_{OSC}) • 100, R_T = 20k		14	20	25	%
Minimum On-Time	BURST Mode, V_{IN} = 12V (Note 6) PULSE SKIP Mode, V_{IN} = 12V (Note 6)			70 60	90 85	ns ns
Minimum Off-Time		●		50	75	ns
SYNC/Mode, Mode Thresholds (Note 5)	High (Rising) Low (Falling)	● ●	 0.14	1.3 0.2	1.7	V V
SYNC/Mode, Clock Thresholds (Note 5)	Rising Falling	● ●	 0.4	1.3 0.8	1.7	V V
f_{SYNC}/f_{OSC} Allowed Ratio	R_T = 20k		0.95	1	1.25	kHz/kHz
SYNC Pin Current	SYNC = 2V SYNC = 0V, Current Out of Pin			10 10	25 25	µA µA
Switch						
Maximum Switch Current Limit Threshold		●	3	3.75	4.65	A
Switch Overcurrent Threshold	Discharges SS Pin			5.6		A
Switch $R_{DS(ON)}$	I_{SW} = 0.5A			100		mΩ
Switch Leakage Current	V_{SW} = 40V			0.1	1	µA
EN/UVLO Logic						
EN/UVLO Pin Threshold (Rising)	Start Switching	●	1.576	1.68	1.90	V
EN/UVLO Pin Threshold (Falling)	Stop Switching	●	1.545	1.6	1.645	V
EN/UVLO Pin Current	$V_{EN/UVLO}$ = 1.6V	●	–75		75	nA
Soft-Start						
Soft-Start Charge Current	SS = 0.5V			2		µA
Soft-Start Pull-Down Resistance	Fault Condition, SS = 0.1V			220		Ω
Error Amplifier						
Error Amplifier Transconductance	FBX = 1.6V FBX = –0.8V			75 60		µA/V µA/V
Error Amplifier Voltage Gain	FBX = 1.6V FBX = –0.8V			185 145		V/V V/V
Error Amplifier Max Source Current	V_C = 1.1V, Current Out of Pin			7		µA
Error Amplifier Max Sink Current	V_C = 1.1V			7		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: $INTV_{CC}$ cannot be externally driven. No additional components or loading is allowed on this pin.

Note 3: The LT8333R is specified over the –40°C to 150°C operating junction range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

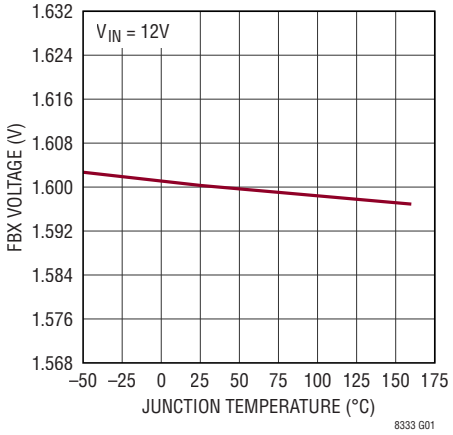
Note 4: The IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

Note 5: For SYNC/MODE inputs required to select modes of operation see the Pin Functions and Applications Information sections.

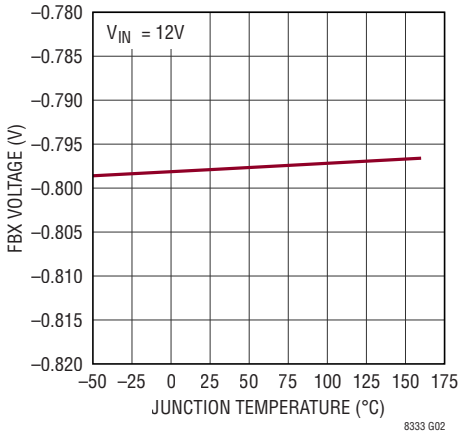
Note 6: The IC is tested in a Boost converter configuration with the output voltage programmed for 12V.

TYPICAL PERFORMANCE CHARACTERISTICS

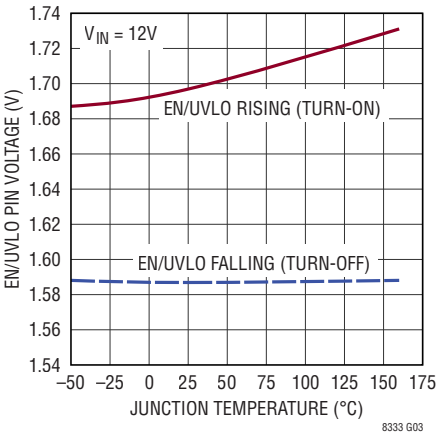
FBX Positive Regulation Voltage vs Temperature



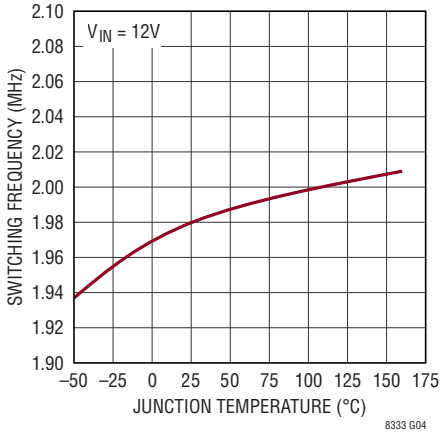
FBX Negative Regulation Voltage vs Temperature



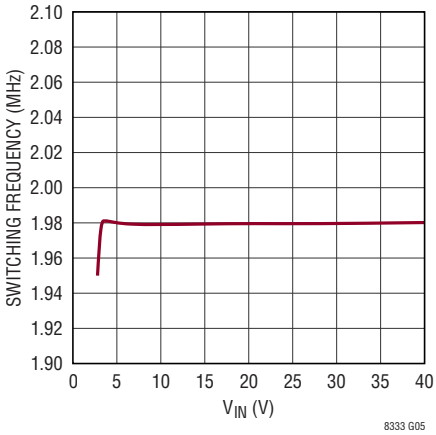
EN/UVLO Pin Thresholds vs Temperature



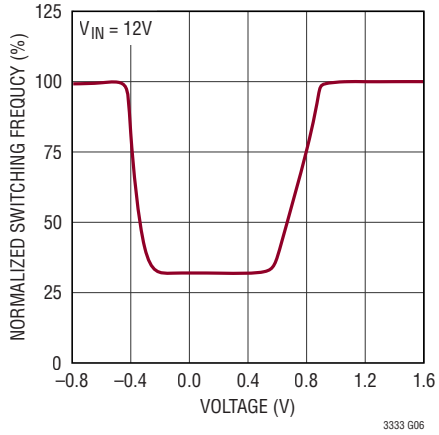
Switching Frequency vs Temperature



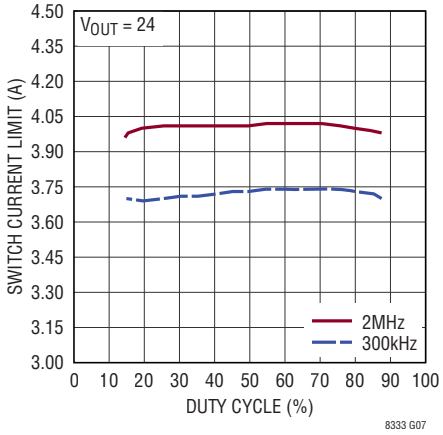
Switching Frequency vs V_{IN}



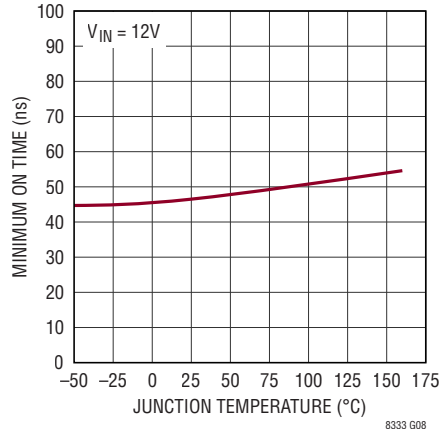
Normalized Switching Frequency vs FBX Voltage



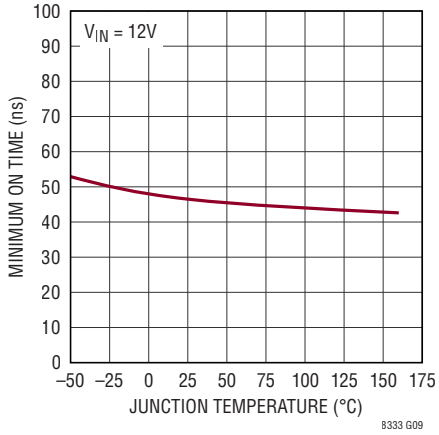
Switch Current Limit vs Duty Cycle



Switch Minimum On-Time vs Temperature

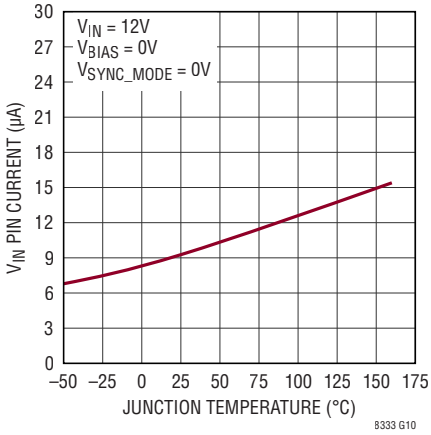


Switch Minimum Off-Time vs Temperature

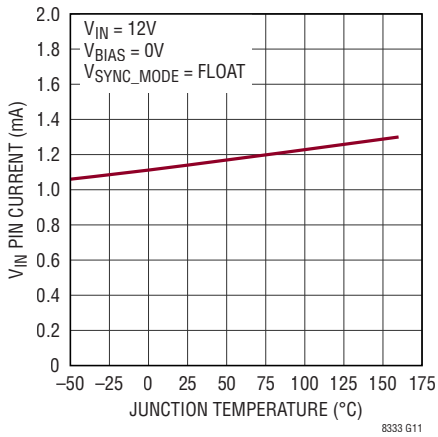


TYPICAL PERFORMANCE CHARACTERISTICS

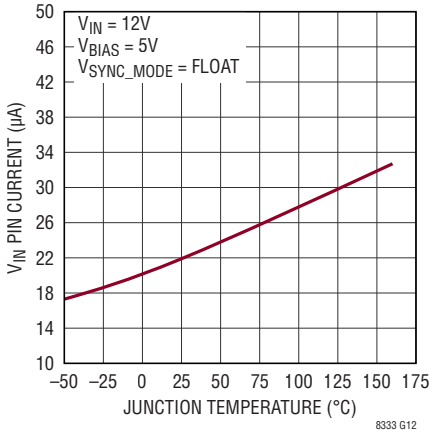
V_{IN} Pin Current (Sleep Mode, Not Switching) vs Temperature



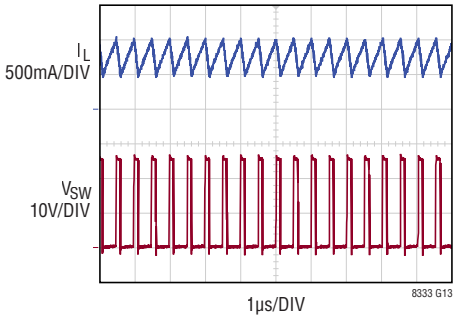
V_{IN} Pin Current (Active Mode, Not Switching, Bias = 0V) vs Temperature



V_{IN} Pin Current (Active Mode, Not Switching, Bias = 5V) vs Temperature

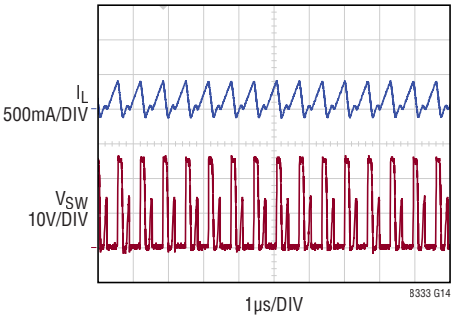


Switching Waveforms (in CCM)



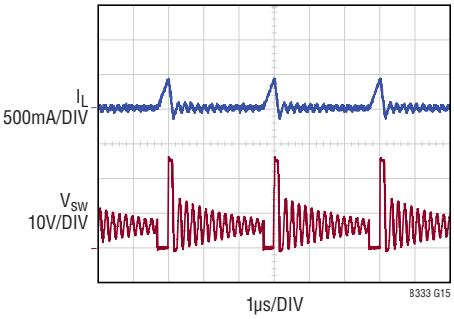
V_{IN} = 6V
V_{OUT} = 24V

Switching Waveforms (in DCM/Light Burst Mode)



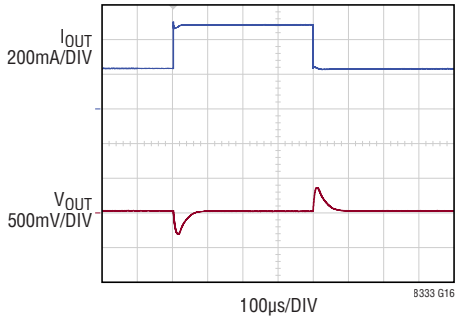
V_{IN} = 6V
V_{OUT} = 24V

Switching Waveforms (in Deep Burst Mode)



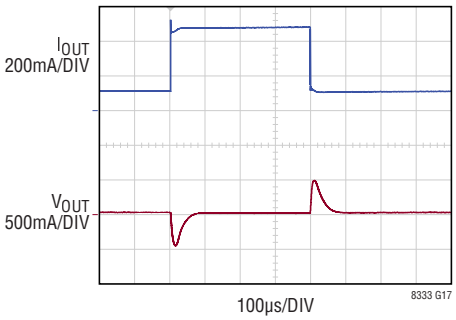
V_{IN} = 6V
V_{OUT} = 24V

V_{OUT} Transient Response: Load Current Transients from 240mA to 480mA to 240mA



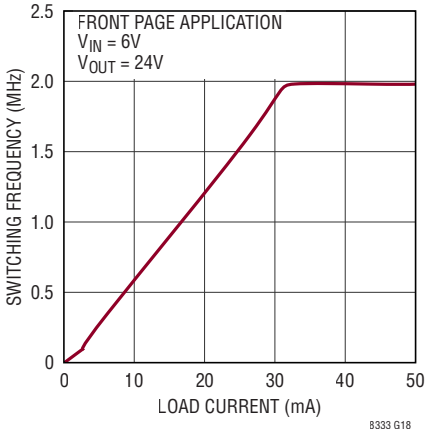
FRONT PAGE APPLICATION
V_{IN} = 5V
V_{OUT} = 24V

V_{OUT} Transient Response: Load Current Transients from 120mA to 480mA to 120mA



FRONT PAGE APPLICATION
V_{IN} = 5V
V_{OUT} = 24V

Burst Frequency vs Load Current



PIN FUNCTIONS

EN/UVLO (Pin 1): Shutdown and Undervoltage Detect Pin. The LT8333 is shut down when this pin is low and active when this pin is high. Below an accurate 1.6V threshold, the part enters undervoltage lockout and stops switching. This allows an undervoltage lockout (UVLO) threshold to be programmed for system input voltage by resistively dividing down system input voltage to the EN/UVLO pin. An 80mV pin hysteresis ensures part switching resumes when the pin exceeds 1.68V. EN/UVLO pin voltage below 0.2V reduces V_{IN} current below 1µA. If shutdown and UVLO features are not required, the pin can be tied directly to system input.

V_{IN} (Pin 2): Input Supply. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pin, and the negative terminal as close as possible to the exposed pad PGND copper (near EN/UVLO).

$INTV_{CC}$ (Pin 3): Regulated 3.2V Supply for Internal Loads. The $INTV_{CC}$ pin must be bypassed with a 1µF low ESR ceramic capacitor to GND. No additional components or loading is allowed on this pin. $INTV_{CC}$ draws power from the BIAS pin if $4.4V \leq BIAS \leq V_{IN}$, otherwise $INTV_{CC}$ is powered by the V_{IN} pin.

BIAS (Pin 4): Second Input Supply for Powering $INTV_{CC}$. Removes the majority of $INTV_{CC}$ current from the V_{IN} pin to improve efficiency when $4.4V \leq BIAS \leq V_{IN}$. If unused, tie the pin to GND.

V_C (Pin 5): Error Amplifier Output Pin. Tie external compensation network to this pin.

FBX (Pin 6): Voltage Regulation Feedback Pin for Positive or Negative Outputs. Connect this pin to a resistor divider between the output and the exposed pad GND copper (near FBX). FBX reduces the switching frequency during start-up and fault conditions when FBX is close to 0V.

RT (Pin 7): A resistor from this pin to the exposed pad GND copper (near FBX) programs switching frequency.

SS (Pin 8): Soft-Start Pin. Connect a capacitor from this pin to GND copper (near FBX) to control the ramp rate of inductor current during converter start-up. SS pin charging current is 2µA. An internal 220Ω MOSFET discharges this pin during shutdown or fault conditions.

SYNC/MODE (Pin 9): This pin allows five selectable modes for optimization of performance.

SYNC/MODE PIN INPUT	CAPABLE MODE(S) OF OPERATION
(1) GND or <0.14V	BURST
(2) External Clock	PULSE-SKIP/SYNC
(3) 100k Resistor to GND	BURST/SSFM
(4) Float (Pin Open)	PULSE-SKIP
(5) $INTV_{CC}$ or >1.7V	PULSE-SKIP/SSFM

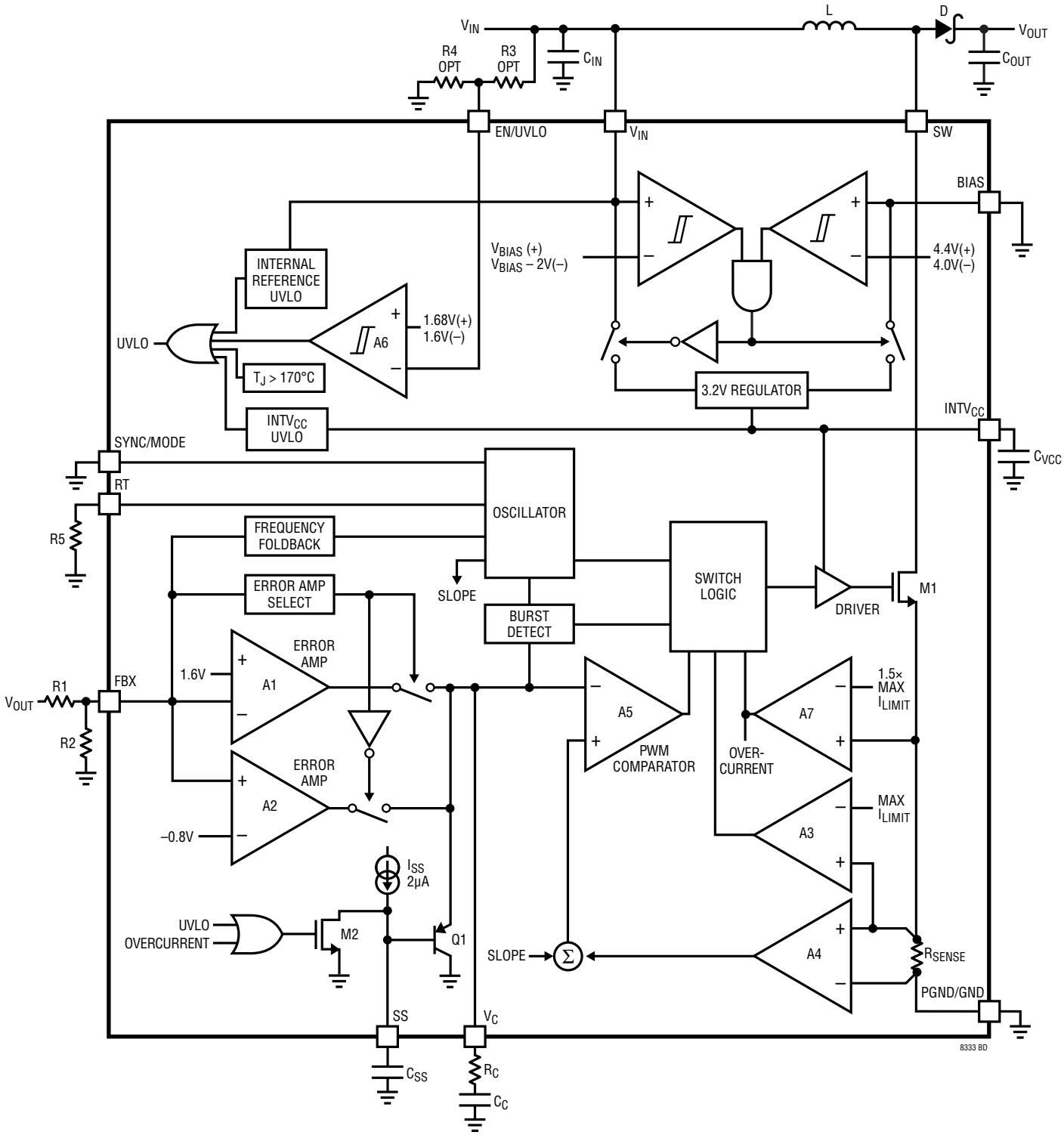
where the selectable modes of operation are:

BURST = low I_Q, low output ripple operation at light loads
PULSE SKIP = skipped pulse(s) at light load (aligned to clock)
SYNC = switching frequency synchronized to external clock
SSFM = spread spectrum frequency modulation for low EMI

SW (Pin 10): Output of the Internal Power Switch. Minimize the metal trace area connected to these pins to reduce EMI.

PGND, GND (Pin 11): Power Ground and Signal Ground for the IC. The package has an exposed pad underneath the IC, which is the best path for heat out of the package. The exposed pad should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT8333. Connect power ground components to the exposed pad copper exiting near the EN/UVLO and SW pins. Connect signal ground components to the exposed pad copper exiting near the V_C and FBX pin.

BLOCK DIAGRAM



OPERATION

The LT8333 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram. An oscillator (with frequency programmed by a resistor at the RT pin) turns on the internal power switch at the beginning of each clock cycle. Current in the inductor then increases until the current comparator trips and turns off the power switch. The peak inductor current at which the switch turns off is controlled by the voltage on the V_C pin. The error amplifier servos the V_C pin by comparing the voltage on the FBX pin with an internal reference voltage (1.60V or 0.80V, depending on the chosen topology). When the load current increases, it causes a reduction in the FBX pin voltage relative to the internal reference. This causes the error amplifier to increase the V_C pin voltage until the new load current is satisfied. In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation. The LT8333 has overvoltage protection as an intrinsic feature of the pulse-skipping and Burst Mode of operation. If V_{OUT} increases above the regulation voltage, this will increase the voltage on the FBX pin above the internal reference voltage. This causes the error amplifier to decrease the V_C pin voltage, which will naturally stop the switching as the part enters a full pulse skip or burst mode idle state.

The LT8333 can generate either positive or negative output voltage with a single FBX pin. It can be configured as a boost or SEPIC converter to generate a positive output voltage, or as an inverting converter to generate a negative output voltage. When configured as a boost converter as shown in the Block Diagram, the FBX pin is pulled up to the internal bias voltage of 1.60V by a voltage divider (R1 and R2) connected from V_{OUT} to GND. Amplifier A2 becomes inactive and amplifier A1 performs (inverting) amplification from FBX to V_C. When the LT8333 is in an inverting configuration, the FBX pin is pulled down to 0.80V by a voltage divider from V_{OUT} to GND. Amplifier A1 becomes inactive and amplifier A2 performs (noninverting) amplification from FBX to V_C.

If the EN/UVLO pin voltage is below 1.6V, the LT8333 enters undervoltage lockout (UVLO), and stops switching. When the EN/UVLO pin voltage is above 1.68V (typical), the LT8333 resumes switching. If the EN/UVLO pin voltage is below 0.2V, the LT8333 draws less than 1µA from V_{IN}.

For the SYNC/MODE pin tied to ground or <0.14V, the LT8333 will enter low output ripple Burst Mode operation for ultralow quiescent current during light loads to maintain high efficiency. For a 100k resistor from SYNC/MODE pin to GND, the LT8333 uses Burst Mode operation for improved efficiency at light loads but seamlessly transitions to Spread Spectrum Modulation of switching frequency for low EMI at heavy loads. For the SYNC/ MODE pin floating (left open), the LT8333 uses pulse-skipping mode, at the expense of hundreds of microamps, to maintain output voltage regulation at light loads by skipping switch pulses. For the SYNC/MODE pin tied to $INTV_{CC}$ or >1.7V, the LT8333 uses pulse-skipping mode and performs Spread Spectrum Modulation of the switching frequency. For the SYNC/MODE pin driven by an external clock, the converter switching frequency is synchronized to that clock and pulse-skipping mode is also enabled. See the Pin Functions section for SYNC/MODE pin.

The LT8333 includes a BIAS pin to improve efficiency across all loads. The LT8333 intelligently chooses between the V_{IN} and BIAS pins to supply the $INTV_{CC}$ for best efficiency. The $INTV_{CC}$ supply current can be drawn from the BIAS pin instead of the V_{IN} pin for $4.4V \le BIAS \le V_{IN}$.

Protection features ensure the immediate disable of switching and reset of the SS pin for any of the following faults: internal reference UVLO, $INTV_{CC}$ UVLO, switch current >1.5 × maximum limit, EN/UVLO < 1.6V or junction temperature > 170°C.

APPLICATIONS INFORMATION

ACHIEVING ULTRALOW QUIESCENT CURRENT

To enhance efficiency at light loads, the LT8333 uses a low ripple Burst Mode architecture. This keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and output ripple. In Burst Mode operation, the LT8333 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode, the LT8333 consumes only 9µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8333 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. To optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current. In addition, all possible leakage currents from the output should also be minimized as they all add to the equivalent output load. The largest contributor to leakage current can be due to the reverse biased leakage of the Schottky diode (see Boost Converter: Diode Selection in this section).

While in Burst Mode operation, the current limit of the switch is approximately 750mA resulting in the output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As the output load ramps upward from zero the switching frequency will increase but only up to the fixed frequency defined by the resistor at the RT pin as shown in Figure 1. The output load at which the LT8333 reaches the fixed frequency varies based on input voltage, output voltage, and inductor choice.

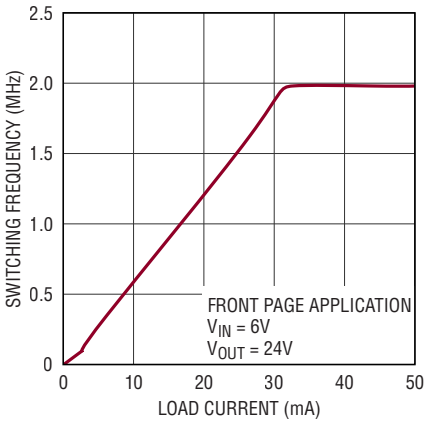


Figure 1. Burst Frequency vs Load Current

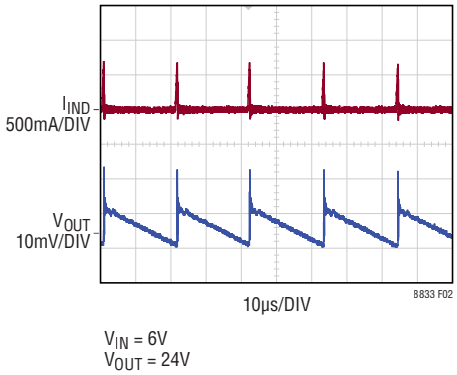


Figure 2. Burst Mode Operation

PROGRAMMING INPUT TURN-ON AND TURN-OFF THRESHOLDS WITH EN/UVLO PIN

The EN/UVLO pin voltage controls whether the LT8333 is enabled or is in a shutdown state. A 1.6V reference and a comparator A6 with built-in hysteresis (typical 80mV) allow the user to accurately program the system input voltage at which the IC turns on and off (see the Block Diagram). The typical input-falling and input-rising threshold voltages can be calculated with Equation 1

$$V_{IN(FALLING,UVLO(-))} = 1.60 \bullet \frac{R3 + R4}{R4}$$
$$V_{IN(RISING,\ UVLO(+))} = 1.68 \bullet \frac{R3 + R4}{R4} \quad (1)$$

V_{IN} current is reduced below 1µA when the EN/UVLO pin voltage is less than 0.2V. The EN/UVLO pin can be connected directly to the input supply V_{IN} for always-enabled operation. A logic input can also control the EN/UVLO pin.

When operating in Burst Mode operation for light load currents, the current through the R3 and R4 network can easily be greater than the supply current consumed by the LT8333. Therefore, R3 and R4 should be large enough to minimize their effect on efficiency at light loads.

$INTV_{CC}$ REGULATOR

A low dropout (LDO) linear regulator, supplied from V_{IN}, produces a 3.2V supply at the $INTV_{CC}$ pin. A minimum 1µF low ESR ceramic capacitor must be used to bypass the $INTV_{CC}$ pin to ground to supply the high transient currents required by the internal power MOSFET gate driver.

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No additional components or loading is allowed on this pin. The $INTV_{CC}$ rising threshold (to allow soft-start and switching) is typically 2.65V. The $INTV_{CC}$ falling threshold (to stop switching and reset soft-start) is typically 2.5V.

To improve efficiency across all loads, the majority of $INTV_{CC}$ current can be drawn from the BIAS pin ($4.4V \leq BIAS \leq V_{IN}$) instead of the V_{IN} pin. For SEPIC applications with V_{IN} often greater than V_{OUT}, the BIAS pin can be directly connected to V_{OUT}. If the BIAS pin is connected to a supply other than V_{OUT}, be sure to bypass the pin with a local ceramic capacitor with a value of at least 1µF

PROGRAMMING SWITCHING FREQUENCY

The LT8333 uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 2MHz by using a resistor tied from the RT pin to ground. Table 1 shows the necessary R_T value for a desired switching frequency.

The R_T resistor required for a desired switching frequency can be calculated with Equation 2.

$$R_T = \frac{51.2}{f_{OSC}} - 5.6 \quad (2)$$

where R_T is in kΩ and fOSC is the desired switching frequency in MHz.

Table 1. SW Frequency vs R_T Value

f_{OSC} (MHz)	R_T (kΩ)
0.3	165
0.45	107
0.75	63.4
1	45.3
1.5	28.7
2	20

Synchronization and Mode Selection

To select low ripple Burst Mode operation, for high efficiency at light loads, tie the SYNC/MODE pin below 0.14V (this can be ground or a logic low output).

To synchronize the LT8333 oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.7V (up to 6V). The LT8333 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LT8333 may be synchronized over a 300kHz to 2MHz range. The RT resistor should be chosen to set the LT8333 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz.

For some applications it is desirable for the LT8333 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. Firstly, the clock stays awake at all times and all switching cycles are aligned to the clock. Secondly, the full switching frequency is maintained at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, float the SYNC pin.

To improve EMI/EMC, the LT8333 can provide spread spectrum frequency modulation (SSFM). This feature varies the clock with a triangle frequency modulation of 20%. For example, if the LT8333's frequency was programmed to switch at 2MHz, spread spectrum mode will modulate the oscillator between 2MHz and 2.4MHz. The 20% modulation will occur at a frequency: $f_{OSC}/256$ where f_{OSC} is the switching frequency programmed using the RT pin.

The LT8333 can also be configured to operate in pulse-skipping/SSFM mode by tying the SYNC/MODE pin above 1.7V. The LT8333 can also be configured for Burst Mode operation at light loads (for improved efficiency) and SSFM at heavy loads (for low EMI) by tying a 100k from the SYNC/MODE pin to GND.

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DUTY-CYCLE CONSIDERATION

The LT8333 minimum on-time, minimum off-time and switching frequency (f_{OSC}) define the allowable minimum and maximum duty cycles of the converter (see Minimum On-Time, Minimum Off-Time, and Switching Frequency in the Electrical Characteristics table and Equation 3).

$$\text{Minimum Allowable Duty Cycle} = \text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$
$$\text{Maximum Allowable Duty Cycle} = 1 - \text{Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)} \quad (3)$$

The required switch duty cycle range for a Boost converter operating in continuous conduction mode (CCM) can be calculated with Equation 4.

$$D_{MIN} = 1 - \frac{V_{IN(MAX)}}{V_{OUT} + V_D}$$
$$D_{MAX} = 1 - \frac{V_{IN(MIN)}}{V_{OUT} + V_D} \quad (4)$$

where V_D is the diode forward voltage drop. If the above duty-cycle calculations for a given application violate the minimum and/or maximum allowed duty cycles for the LT8333, operation in discontinuous conduction mode (DCM) might provide a solution. For the same V_{IN} and V_{OUT} levels, operation in DCM does not demand as low a duty cycle as in CCM. DCM also allows higher duty-cycle operation than CCM. The additional advantage of DCM is the removal of the limitations to inductor value and duty cycle required to avoid subharmonic oscillations and the right half plane zero (RHPZ). While DCM provides these benefits, the trade-off is higher inductor peak current, lower available output power and reduced efficiency.

SETTING THE OUTPUT VOLTAGE

The output voltage is programmed with a resistor divider from the output to the FBX pin. Choose the resistor values for a positive output voltage according to Equation 5.

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{1.6V} - 1\right) \quad (5)$$

Choose the resistor values for a negative output voltage according to Equation 6.

$$R1 = R2 \bullet \left(\frac{|V_{OUT}|}{0.8V} - 1\right) \quad (6)$$

The locations of R1 and R2 are shown in the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

Higher value FBX divider resistors result in the lowest input quiescent current and highest light-load efficiency. FBX divider resistors R1 and R2 are usually in the range from 25k to 1Ms.

SOFT-START

The LT8333 contains several features to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The LT8333 addresses this mechanism with a programmable soft-start function. As shown in the Block Diagram, the soft-start function controls the ramp of the power switch current by controlling the ramp of V_C through Q1. This allows the output capacitor to be charged gradually toward its final value while limiting the start-up peak currents. Figure 3 shows the output voltage and supply current for the front page Typical Application. It shows that both the output voltage and supply current come up gradually.

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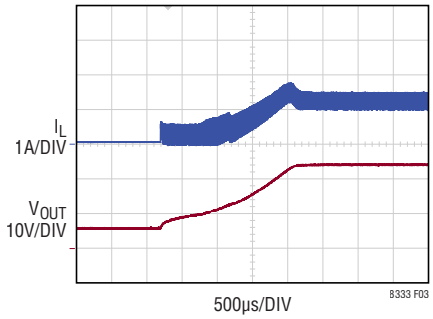

Figure 3. Soft-Start Waveforms

FAULT PROTECTION

An inductor overcurrent fault (> 5.6A) and/or $INTV_{CC}$ undervoltage ($INTV_{CC}$ < 2.5V) and/or thermal lockout (T_J > 170°C) will immediately prevent switching, will reset the SS pin and will pull down V_C. Once all faults are removed, the LT8333 will soft-start V_C and hence inductor peak current.

FREQUENCY FOLDBACK

During start-up or fault conditions in which V_{OUT} is very low, extremely small duty cycles may be required to maintain control of inductor peak current. The minimum on-time limitation of the power switch might prevent these low duty cycles from being achievable. In this scenario, inductor current rise will exceed inductor current fall during each cycle, causing inductor current to "walk up" beyond the switch current limit. The LT8333 provides protection from this by folding back switching frequency whenever FBX or SS pins are close to GND (low V_{OUT} levels or start-up). This frequency foldback provides a larger switch-off time, allowing inductor current to fall enough each cycle (see Normalized Switching Frequency vs FBX Voltage in the Typical Performance Characteristics section).

THERMAL LOCKOUT

If the LT8333 die temperature reaches 170°C (typical), the part will stop switching and go into thermal lockout. When the die temperature has dropped by 5°C (nominal), the part will resume switching with a soft-started inductor peak current.

COMPENSATION

Loop compensation determines the stability and transient performance. The LT8333 uses current mode control to regulate the output, which simplifies loop compensation. The optimum values depend on the converter topology, the component values, and the operating conditions (including the input voltage, load current, etc.). To compensate the feedback loop of the LT8333, a series resistor-capacitor network is usually connected from the V_C pin to GND. The Block Diagram shows the typical V_C compensation network. For most applications, the capacitor should be in the range of 100pF to 10nF, and the resistor should be in the range of 5k to 100k. A small capacitor is often connected in parallel with the RC compensation network to attenuate the V_C voltage ripple induced from the output voltage ripple through the internal error amplifier. The parallel capacitor usually ranges in value from 2.2pF to 22pF. A practical approach to designing the compensation network is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. Application Note 76 is a good reference.

THERMAL CONSIDERATIONS

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8333. The DFN package has an exposed pad underneath the IC, which is the best path for heat out of the package. The exposed pad should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT8333. The ground plane should be connected to large copper layers to spread heat dissipated by the LT8333. Power dissipation within the LT8333 (PDISS_LT8333) can be estimated by subtracting the inductor and Schottky diode power losses from the total power losses calculated in an efficiency measurement. The junction temperature of LT8333 can then be estimated with Equation 7.

$$T_J(LT8333) = T_A + \theta_{JA} \bullet P_{DISS\_LT8333} \quad (7)$$

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APPLICATION CIRCUITS

The LT8333 can be configured for different topologies. The first topology analyzed will be the boost converter, followed by the SEPIC and inverting converters.

Boost Converter: Switch Duty Cycle

The LT8333 can be configured as a boost converter for the applications where the converter output voltage is higher than the input voltage. Remember that boost converters are not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the SEPIC Converter Applications later in this section.

The conversion ratio as a function of duty cycles is given by Equation 8.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D} \quad (8)$$

in continuous conduction mode (CCM).

For a boost converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage (Equation 9).

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}} \quad (9)$$

Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency at the cost of reduced efficiencies, higher switching currents, and lower available output power.

Boost Converter: Maximum Output Current Capability and Inductor Selection

For the boost topology, the maximum average inductor current is given by Equation 10.

$$I_{L(MAX)(AVG)} = I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}} \bullet \frac{1}{\eta} \quad (10)$$

where η (< 1.0) is the converter efficiency.

Due to the current limit of its internal power switch, the LT8333 should be used in a boost converter whose maximum output current ($I_{O(MAX)}$) is given by Equation 11.

$$I_{O(MAX)} \leq \frac{V_{IN(MIN)}}{V_{OUT}} \bullet \left(3A - 0.5 \bullet \Delta I_{SW}\right) \bullet \eta \quad (11)$$

Minimum possible inductor value and switching frequency should also be considered since they will increase inductor ripple current ΔI_{SW}.

The inductor ripple current ΔI_{SW} has a direct effect on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of ΔI_{SW} increases output current capability but requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_{SW} provides fast transient response and allows the use of low inductances but results in higher input current ripple and greater core losses and reduces output current capability. It is recommended to choose a ΔI_{SW} of approximately 1.1A.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined with Equation 12.

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX} \quad (12)$$

The peak inductor current is the switch current limit (maximum 4.7A), and the RMS inductor current is approximately equal to $I_{L(MAX)(AVG)}$.

Choose an inductor that can handle at least 4.7A without saturating and ensure that the inductor has a low DCR (copper wire resistance) to minimize I^2R power losses. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one-half of the total switch current. For better efficiency, use similar valued inductors with a larger volume. Many different sizes and shapes are available from various manufacturers (see Table 2). Choose a core material that has low losses at the programmed switching frequency, such as a ferrite core. The final value chosen for the inductor

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should not allow peak inductor currents to exceed 3A in steady state at maximum load. Due to tolerances, be sure to account for minimum possible inductance value, switching frequency and converter efficiency.

For inductor current operation in CCM and duty cycles above 50%, the LT8333's internal slope compensation prevents sub-harmonic oscillations provided the inductor value exceeds a minimum value given by Equation 13.

$$L > \frac{V_{IN}}{\left(-21 \bullet D^2 + 31.5 \bullet D - 7.5\right) \bullet \left(f_{OSC}\right)} \bullet \frac{(2 \bullet D - 1)}{(1 - D)} \quad (13)$$

Lower L values are allowed if the inductor current operates in DCM or duty-cycle operation is below 50%.

Table 2. Inductor Manufacturers

Sumida	www.sumida.com
TDK	www.tdk.com
Murata	www.murata.com
Coilcraft	www.coilcraft.com
Wurth	www.we-online.com

BOOST CONVERTER: INPUT CAPACITOR SELECTION

Bypass the input of the LT8333 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pins. Y5V types should not be used due to poor performance over temperature and applied voltage. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT8333 and will easily handle the ripple current. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8333. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8333 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8333's voltage rating. This situation is easily avoided (see Application Note 88).

BOOST CONVERTER: OUTPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they are small and have extremely low ESR. Use X5R or X7R types. This choice will provide low output ripple and good transient response. A 4.7µF to 47µF output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1µF or 2.2µF output capacitor. Solid tantalum or OS-CON capacitor can be used, but they will occupy more board area than a ceramic and will have a higher ESR. Always use a capacitor with a sufficient voltage rating.

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct output capacitors for a given output ripple voltage. The effect of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform for a typical boost converter is illustrated in Figure 4.

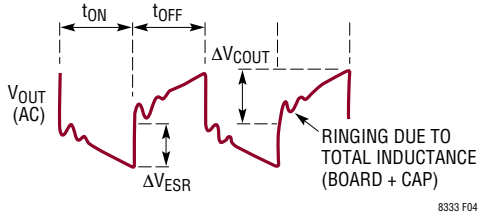

Figure 4. The Output Ripple Waveform of a Boost Converter

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step ΔV_{ESR} and the charging/discharging ΔV_{COUT}. For simplicity, we will choose 2% for the maximum output ripple, to be divided equally between ΔV_{ESR} and ΔV_{COUT}. This percentage ripple will change, depending on the requirements of the application, and the following equations can easily be modified. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined with Equation 14.

$$ESR_{COUT} \leq \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}} \quad (14)$$

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For the bulk C component, which also contributes 1% to the total ripple is given by Equation 15.

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet V_{OUT} \bullet f_{OSC}} \quad (15)$$

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 4. The RMS ripple current rating of the output capacitor can be determined with Equation 16.

$$I_{RMS(COUT)} \geq I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (16)$$

Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors in parallel are commonly used to reduce the effect of parasitic inductance in the output capacitor, which reduces high frequency switching noise on the converter output.

CERAMIC CAPACITORS

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8333 due to their piezoelectric nature. When in Burst Mode operation, the LT8333's switching frequency depends on the load current, and at very light loads the LT8333 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8333 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 3. Ceramic Capacitor Manufacturers

Taiyo Yuden	www.ty-top.com
AVX	www.avx.com
Murata	www.murata.com
TDK	www.tdk.com

BOOST CONVERTER: DIODE SELECTION

A Schottky diode is recommended for use with the LT8333. Low leakage Schottky diodes are necessary when low quiescent current is desired at low loads. The diode leakage appears as an equivalent load at the output and should be minimized. Choose Schottky diodes with sufficient reverse voltage ratings for the target applications.

Table 4. Recommended Schottky Diodes

PART NUMBER	AVERAGE FORWARD CURRENT (A)	REVERSE VOLTAGE (V)	REVERSE CURRENT (µA)	MANUFACTURER
DFLS260	2	60	100	Diodes, Inc.
PMEG4020EPA	2	40	20	Nexperia
PMEG3020EPA	2	30	435	Nexperia
PMEG3020ER	2	30	600	Nexperia

BOOST CONVERTER: LAYOUT HINTS

The high-speed operation of the LT8333 demands careful attention to board layout. Careless layout will result in performance degradation. Figure 5 shows the recommended component placement for a boost converter. Note the vias under the exposed pad. These should connect to a local ground plane for better thermal performance.

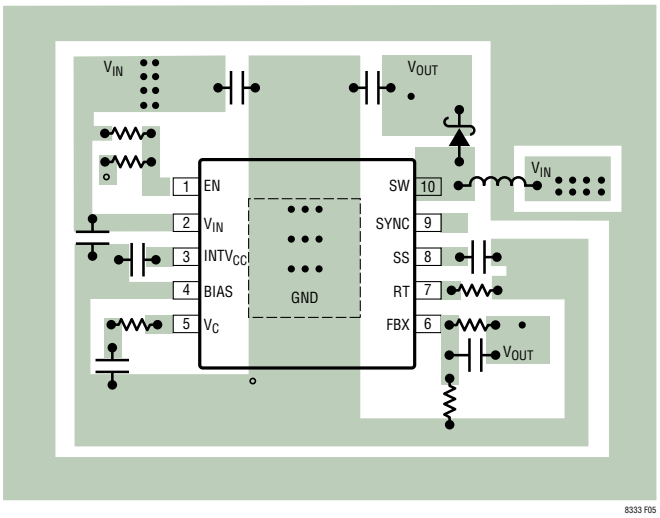

Figure 5. Suggested Boost Converter Layout

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SEPIC CONVERTER APPLICATIONS

The LT8333 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 6. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is given by Equation 17.

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{D}{1 - D} \quad (17)$$

in continuous conduction mode (CCM).

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

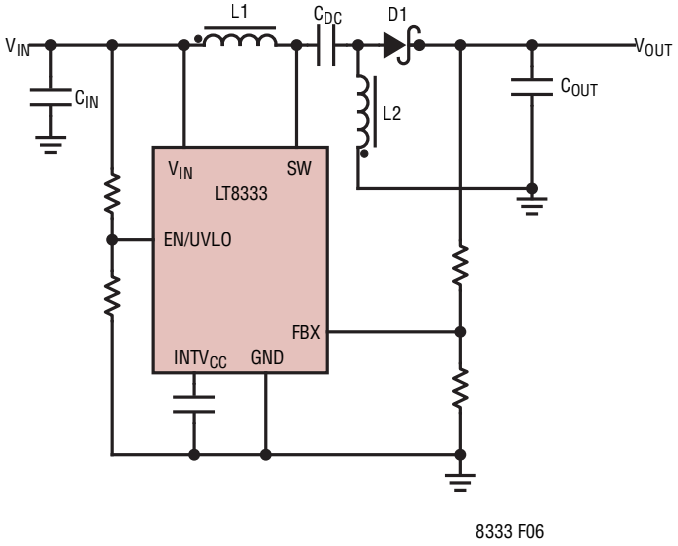

Figure 6. LT8333 Configured in a SEPIC Topology

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}) and the diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter operates at the minimum input voltage (Equation 18).

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_{OUT} + V_D} \quad (18)$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage (Equation 19).

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{IN(MAX)} + V_{OUT} + V_D} \quad (19)$$

Be sure to check that D_{MAX} and D_{MIN} obey Equation 20.

$$D_{MAX} < 1 - \text{Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$
$$\text{and} \quad (20)$$
$$D_{MIN} > \text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

where Minimum Off-Time, Minimum On-Time and f_{OSC} are specified in the Electrical Characteristics table.

SEPIC Converter: The Maximum Output Current Capability and Inductor Selection

As shown in Figure 6, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 may be independent but can also be wound on the same core since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact, that ideally the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are given by Equation 21.

$$I_{L1(MAX)(AVG)} = I_{IN(MAX)(AVG)} = I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}} \quad (21)$$
$$I_{L2(MAX)(AVG)} = I_{O(MAX)}$$

In a SEPIC converter, the switch current is equal to $I_{L1} + I_{L2}$ when the power switch is on, therefore, the maximum average switch current is defined with Equation 22.

$$I_{SW(MAX)(AVG)} = I_{L1(MAX)(AVG)} + I_{L2(MAX)(AVG)}$$
$$= I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}} \quad (22)$$

and the peak switch current is give by Equation 23.

$$I_{SW(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}} \quad (23)$$

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The constant χ in the preceding equations represents the percentage peak-to-peak ripple current in the switch, relative to $I_{SW(MAX)(AVG)}$, as shown in Figure 7. Then, the switch ripple current ΔI_{SW} can be calculated with Equation 24.

$$\Delta I_{SW} = \chi \bullet I_{SW(MAX)(AVG)} \quad (24)$$

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical (Equation 25).

$$\Delta I_{L1} = \Delta I_{L2} = 0.5 \bullet \Delta I_{SW} \quad (25)$$

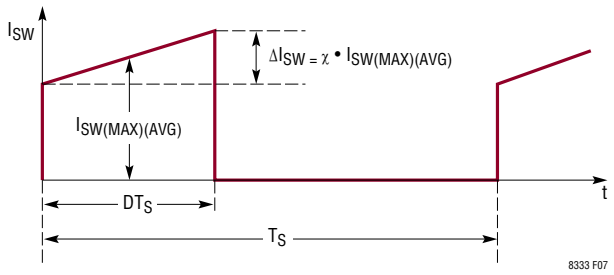


Figure 7. The Switch Current Waveform of the SEPIC Converter

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L allows the use of low inductances but results in higher input current ripple and greater core losses. It is recommended that χ falls in the range of 0.5 to 0.8.

Due to the current limit of its internal power switch, the LT8333 should be used in a SEPIC converter whose maximum output current ($I_{O(MAX)}$) is given by Equation 26.

$$I_{O(MAX)} < (1 - D_{MAX}) \bullet (3A - 0.5 \bullet \Delta I_{SW}) \bullet \eta \quad (26)$$

where η (<1.0) is the converter efficiency. Minimum possible inductor value and switching frequency should also be considered since they will increase inductor ripple current ΔI_{SW}.

Given an operating input voltage range, and having chosen ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined with Equation 27.

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \bullet \Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX} \quad (27)$$

For most SEPIC applications, the equal inductor values will fall in the range of 2.2µH to 100µH.

By making L1 = L2, and winding them on the same core, the value of inductance in the Equation 27 is replaced by 2L, due to mutual inductance (Equation 28).

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX} \quad (28)$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are given by Equation 29.

$$I_{L1(PEAK)} = I_{L1(MAX)} + 0.5 \bullet \Delta I_{L1}$$
$$I_{L2(PEAK)} = I_{L2(MAX)} + 0.5 \bullet \Delta I_{L2} \quad (29)$$

The maximum RMS inductor currents are approximately equal to the maximum average inductor currents.

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

Similar to Boost converters, the SEPIC converter also needs slope compensation to prevent subharmonic oscillations while operating in CCM. The Equation 9 presented in the SEPIC Converter Applications section defines the minimum inductance value to avoid subharmonic oscillations when coupled inductors are used. For uncoupled inductors, the minimum inductance requirement is doubled.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current.

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than $V_{OUT} + V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient). The power dissipated by the diode is given by Equation 30.

$$P_D = I_{O(MAX)} \bullet V_D \quad (30)$$

APPLICATIONS INFORMATION

where V_D is diode's forward voltage drop, and the diode junction temperature is given by Equation 31.

$$T_J = T_A + P_D \bullet R\theta_{JA} \quad (31)$$

The $R\theta_{JA}$ used in this equation normally includes the $R\theta_{JC}$ for the device, plus the thermal resistance from the board, to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the inductor, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC converter sections.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (CDC, as shown in Figure 6) should be larger than the maximum input voltage (Equation 32).

$$V_{CDC} > V_{IN(MAX)} \quad (32)$$

CDC has nearly a rectangular current waveform. During the switch off-time, the current through CDC is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined with Equation 33.

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}} \quad (33)$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for CDC.

INVERTING CONVERTER APPLICATIONS

The LT8333 can be configured as a dual-inductor inverting topology, as shown in Figure 8. The V_{OUT} to V_{IN} ratio is given by Equation 34.

$$\frac{|V_{OUT}| + V_D}{V_{IN}} = \frac{D}{1 - D} \quad (34)$$

in continuous conduction mode (CCM)

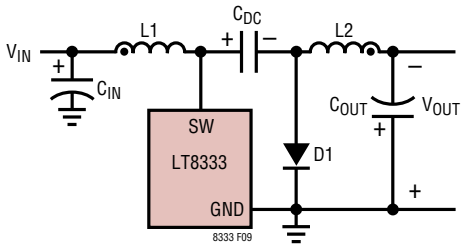


Figure 8. A Simplified Inverting Converter

Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage (V_{OUT}) and the input voltage (V_{IN}).

The maximum duty cycle (DMAX) occurs when the converter has the minimum input voltage (Equation 35).

$$D_{MAX} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MIN)}} \quad (35)$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage (Equation 36).

$$D_{MIN} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MAX)}} \quad (36)$$

Be sure to check that D_{MAX} and D_{MIN} obey Equation 37.

$$D_{MAX} < 1 - \text{Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$
$$\text{and} \quad (37)$$
$$D_{MIN} > \text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

where Minimum Off-Time, Minimum On-Time and f_{OSC} are specified in the Electrical Characteristics table.

Inverting Converter: Inductor, Output Diode and Input Capacitor Selections

The selections of the inductor, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC converter sections.

APPLICATIONS INFORMATION

Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost, flyback and SEPIC converters for similar output ripples. This is because in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor (Equation 38).

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \bullet \left(ESR_{COUT} + \frac{1}{8 \bullet f_{OSC} \bullet C_{OUT}} \right) \quad (38)$$

After specifying the maximum output ripple, the user can select the output capacitors according to E38..

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than (Equation 39).

$$I_{RMS(COUT)} > 0.3 \bullet \Delta I_{L2} \quad (39)$$

Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (CDC, as shown in Figure 8) should be larger than the maximum input voltage minus the output voltage (negative voltage), Equation 40.

$$V_{CDC} > V_{IN(MAX)} + |V_{OUT}| \quad (40)$$

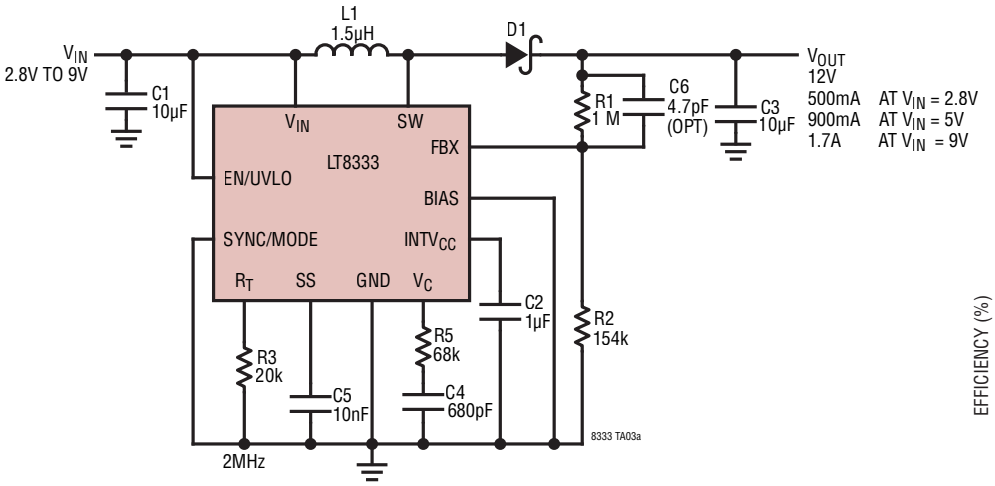
CDC has nearly a rectangular current waveform. During the switch off-time, the current through CDC is I_{IN}, while approximately I_O flows during the on-time. The RMS rating of the coupling capacitor is determined with Equation 41.

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (41)$$

where Minimum Off-Time, Minimum On-Time and f_{OSC} A low ESR and ESL, X5R or X7R ceramic capacitor works well for CDC.

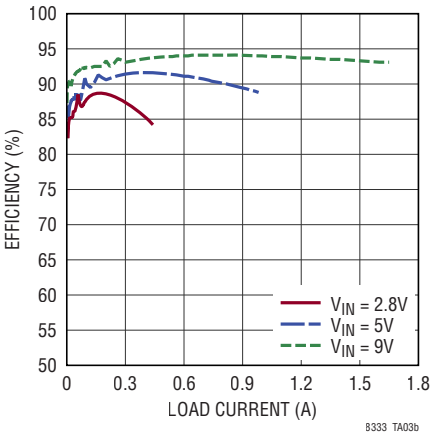
TYPICAL APPLICATION

2MHz, 2.8V to 9V Input, 12V Output Boost Converter

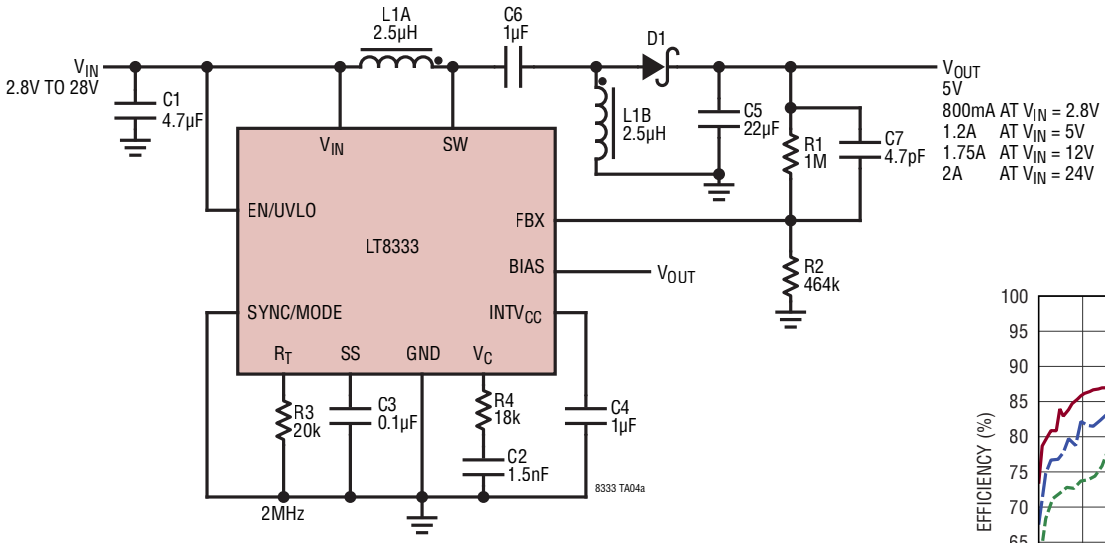


D1: NEXPERIA PMEG4020EPA
L1: COILCRAFT XGL4020-152MEC
C1, C3: MLCC, 1206 or 1210, X7R, 50V

Efficiency

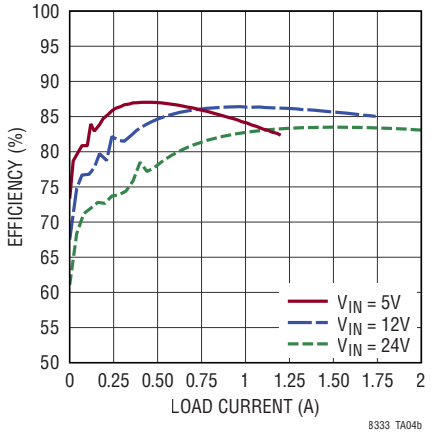


2MHz, 2.8V to 28V Input, 5V SEPIC Converter



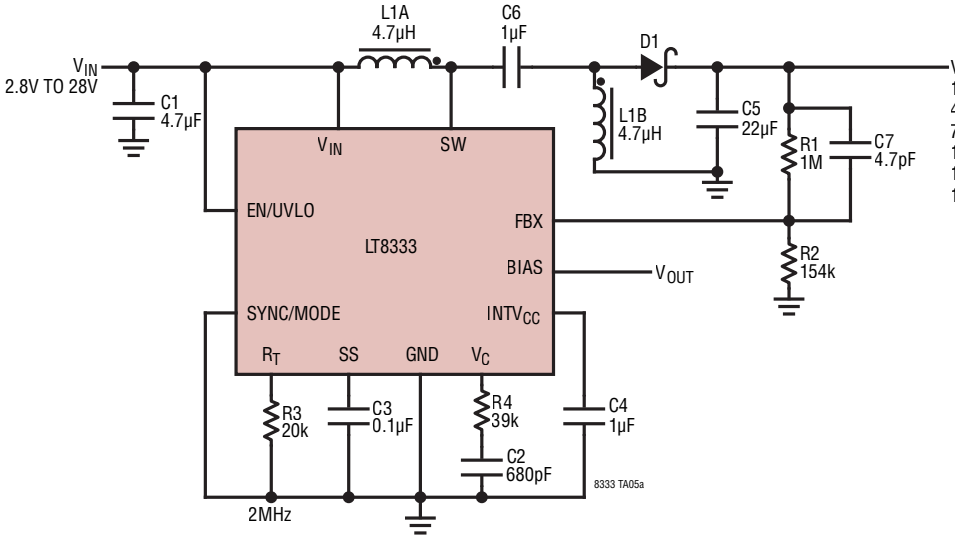
D1: NEXPERIA PMEG4020EPA
C6: TDK CGJ4J3X7R1H105K125AB
L1A, L1B COILCRAFT MSD7342-252MLB

Efficiency



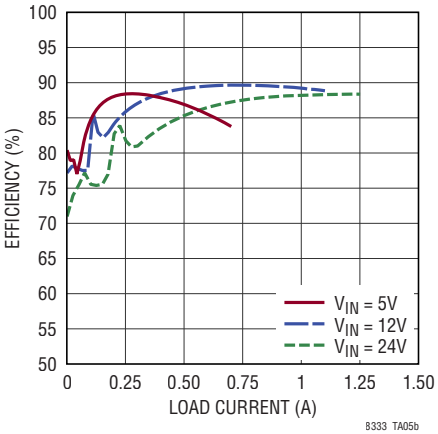
TYPICAL APPLICATION

2MHz, 2.8V to 28V Input, 12V SEPIC Converter

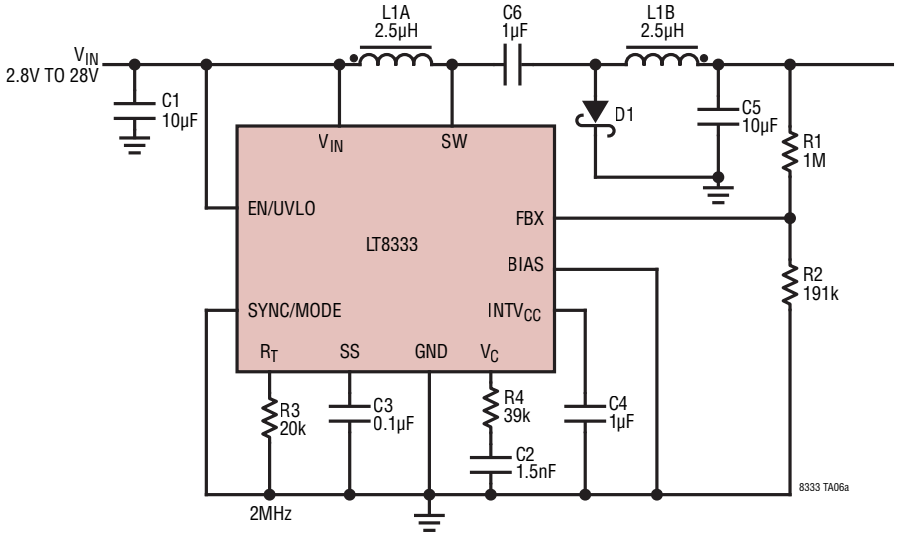


D1: NEXPERIA PMEG4020EPA
C6: TDK CGJ4J3X7R1H105K125AB
L1A, L1B COILCRAFT MSD7342-472MLB

Efficiency

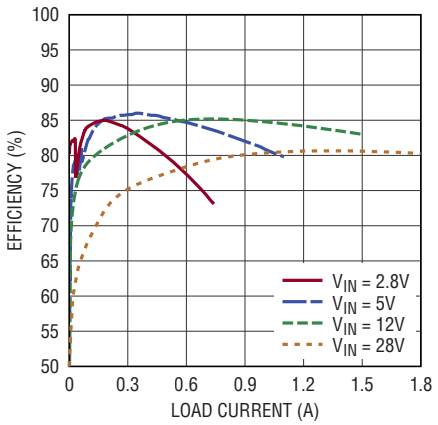


2MHz, 2.8V to 28V Input, –5V Inverting Converter



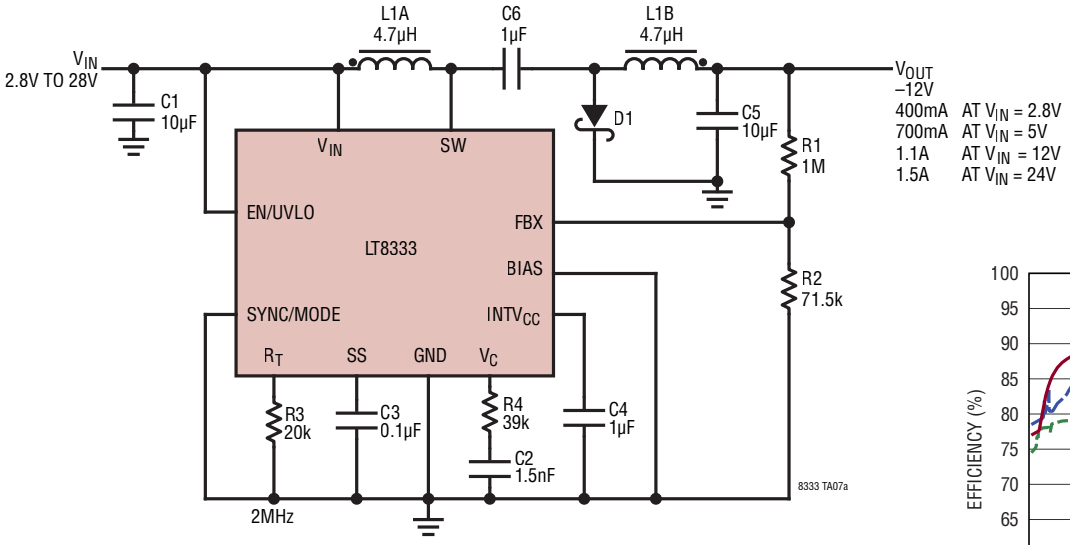
D1: NEXPERIA PMEG3020ER
C6: TDK CGJ4J3X7R1H105K125AB
L1A, L1B COILCRAFT MSD7342-252MLB

Efficiency



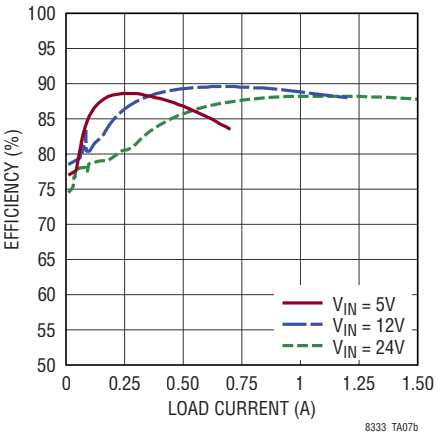
TYPICAL APPLICATION

2MHz, 2.8V to 28V Input, –12V Inverting Converter



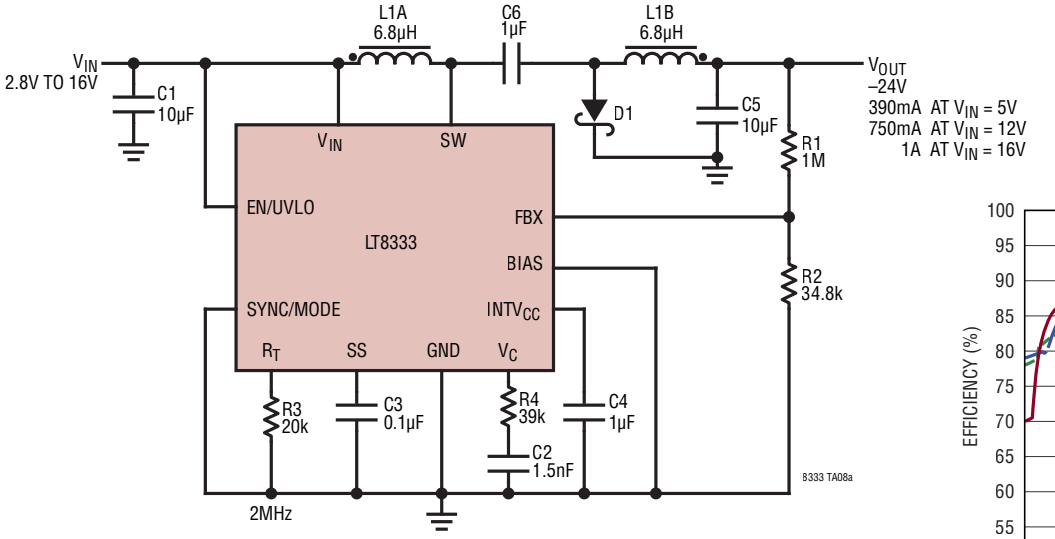
D1: NEXPERIA PMEG4020EPA
C6: TDK CGJ4J3X7R1H105K125AB
L1A, L1B COILCRAFT MSD7342-472MLB

Efficiency



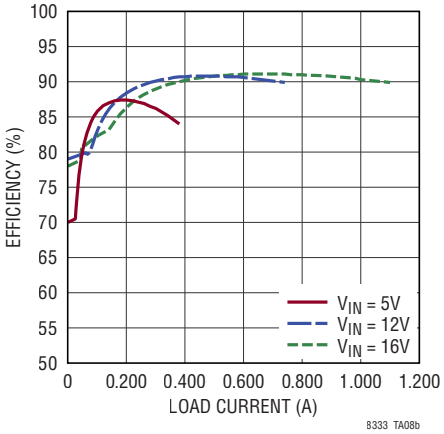
TYPICAL APPLICATION

2MHz, 2.8V to 16V Input, –24V Inverting Converter



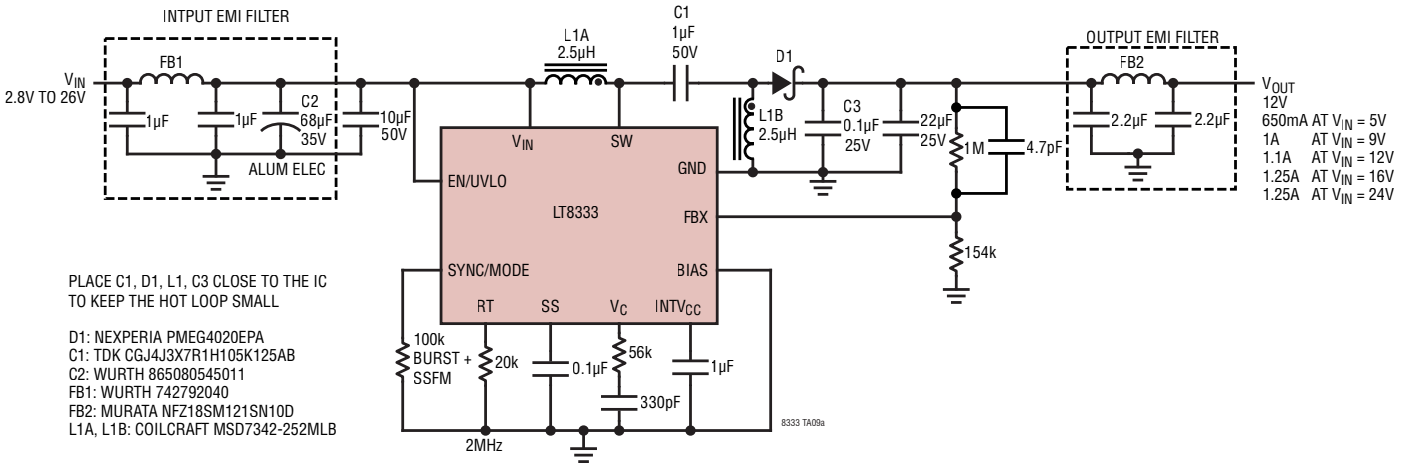
D1: NEXPERIA PMEG4020EPA
C6: TDK CGJ4J3X7R1H105K125AB
L1A, L1B COILCRAFT MSD7342-682MLB

Efficiency

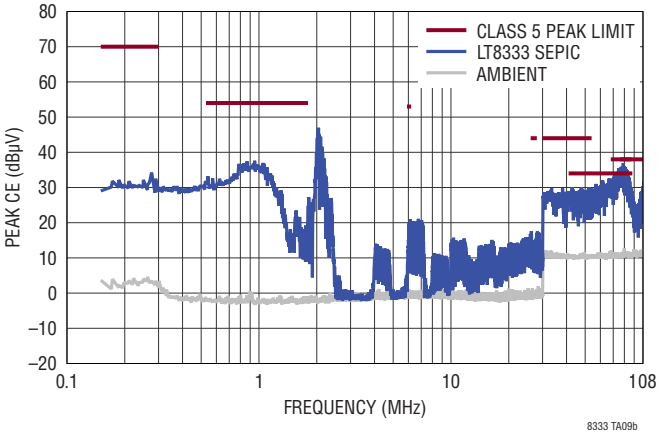


TYPICAL APPLICATION

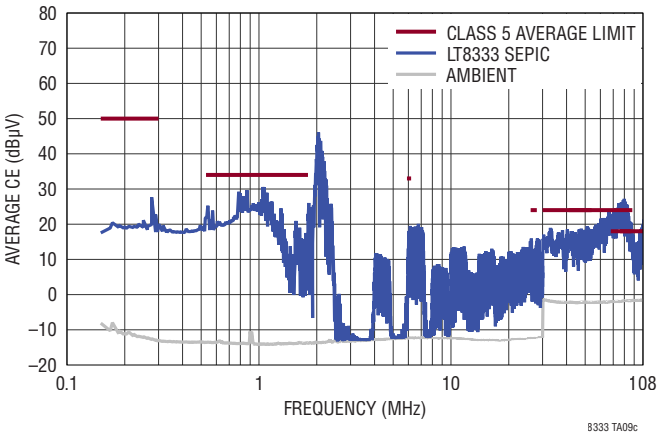
Low I_Q, Low EMI 2MHz, 12V Output SEPIC Converter with SSFM



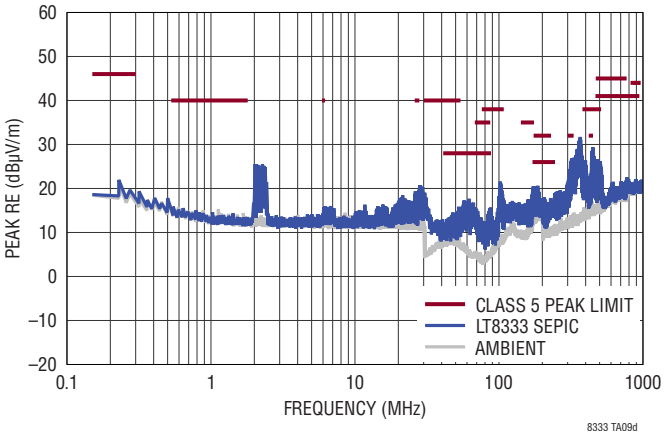
CISPR25 Conducted Emission Performance Voltage Method



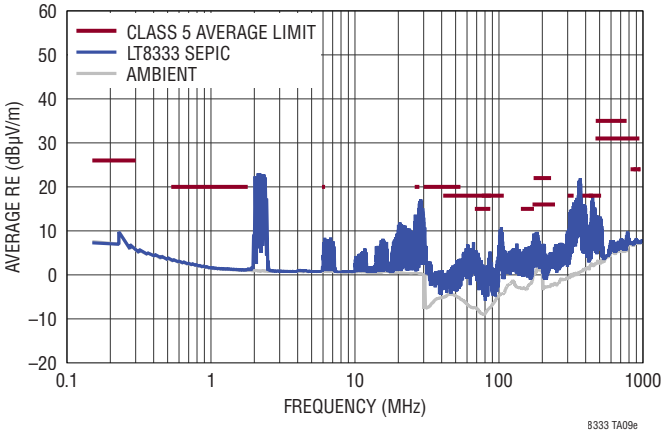
CISPR25 Conducted Emission Performance Voltage Method



CISPR25 Radiated EMI Performance

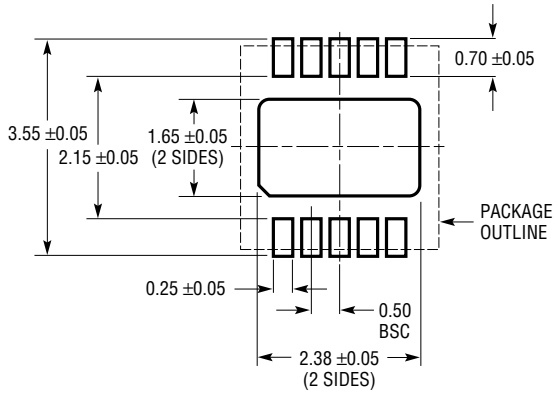


CISPR25 Radiated EMI Performance

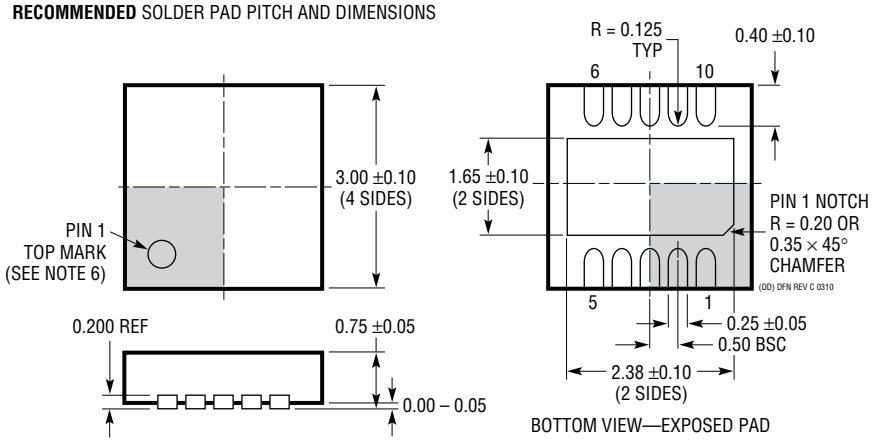


PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

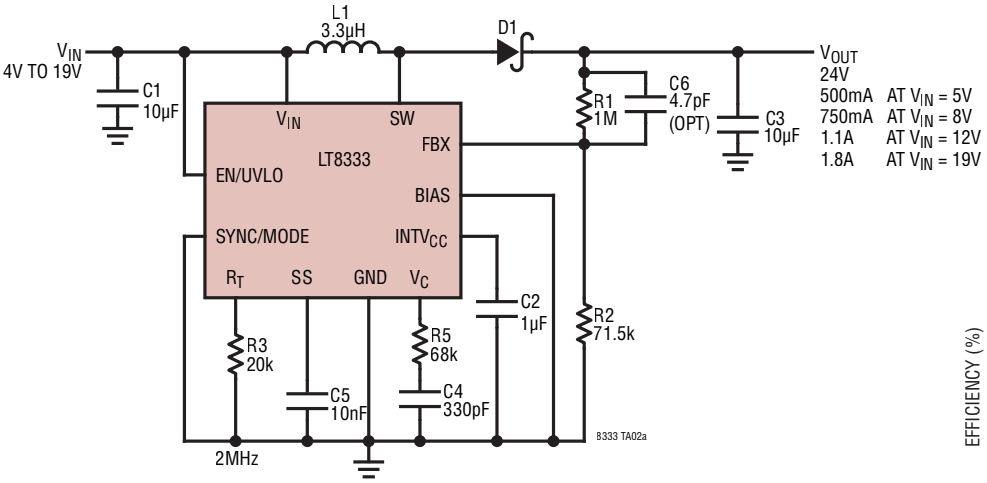


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

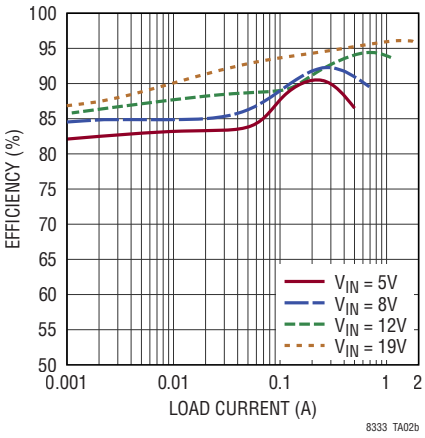
TYPICAL APPLICATION

2MHz, 4V to 19V Input, 24V Output Boost Converter



D1: NEXPERIA PMEG3020EPA
L1: COILCRAFT XGL4020-332MEC
C1,C3: MLCC, 1206 or 1210, X7R, 50V

Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8300	100V_{IN} Micropower Isolated Flyback Converter with 150V/260mA Switch	V_{IN} = 6V to 100V, Low I_Q Monolithic No-Opto Flyback, 5-Lead TSOT-23 Package
LT8330	60V, 1A, Low I_Q Boost/SEPIC/Inverting 2MHz Converter	V_{IN} = 3V to 40V, $V_{OUT(MAX)}$ = 60V, I_Q = 6µA (Burst Mode Operation), 6-Lead TSOT-23 and 3mm × 2mm DFN Packages
LT8331	Low I_Q Boost/SEPIC/Flyback/Inverting Converter with 140V/0.5A Switch	V_{IN} = 4.5V to 100V, $V_{OUT(MAX)}$ =140V, I_Q = 6µA (Burst Mode Operation), MSOP-16(12)E Package
LT8334	Low I_Q Boost/SEPIC/Inverting Converter with 5A, 40V Switch	V_{IN} = 2.8V to 40V, $V_{OUT(MAX)}$ = 40V, I_Q = 9µA (Burst Mode Operation), 4mm × 3mm DFN Package
LT8335	28V, 2A, Low IQ Boost/SEPIC/Inverting 2MHz Converter	V_{IN} = 3V to 25V, $V_{OUT(MAX)}$ = 25V, I_Q = 6µA (Burst Mode Operation), 3mm × 2mm DFN Package
LT8362	Low I_Q Boost/SEPIC/Inverting Converter with 2A, 60V Switch	V_{IN} = 2.8V to 60V, $V_{OUT(MAX)}$ = 60V, I_Q = 9µA (Burst Mode Operation), 12-Lead MSE16 and 3mm × 3mm DFN Packages
LT8364	Low I_Q Boost/SEPIC/Inverting Converter with 4A, 60V Switch	V_{IN} = 2.8V to 60V, $V_{OUT(MAX)}$ = 60V, I_Q = 9µA (Burst Mode Operation), 12-Lead MSE16 and 4mm × 3mm DFN Packages
LT8494	70V, 2A Boost/SEPIC 1.5MHz High Efficiency Step-Up DC/DC Converter	V_{IN} = 1V to 60V (2.5V to 32V Start-Up), $V_{OUT(MAX)}$ = 70V, I_Q = 3µA (Burst Mode Operation), I_{SD} <1µA, 20-Lead TSSOP Package
LT8570/LT8570-1	65V, 500mA/250mA Boost/Inverting DC/DC Converter	$V_{IN(MIN)}$ = 2.55V, $V_{IN(MAX)}$ = 40V, $V_{OUT(MAX)}$ = ±60V, I_Q = 1.2mA, I_{SD} <1mA, 3mm × 3mm DFN-8 and MSOP-8E Packages
LT8580	1A (I_{SW}), 65V, 1.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.55V to 40V, $V_{OUT(MAX)}$ = 65V, I_Q = 1.2mA, I_{SD} <1µA, 3mm × 3mm DFN-8, and MSOP-8E Package