Evaluating the ADAQ23876/ADAQ23878 16-/18-Bit, 15 MSPS, µModule Data Acquisition Solutions

FEATURES

- Evaluation boards for ADAQ23876 and ADAQ23878, 16-/18-bit, 15 MSPS, µModule data acquisition solutions
- Versatile analog signal conditioning circuitry
- On-board reference, LDO, and power supply circuits
- PC software for control and data analysis of time and frequency domain
- System demonstration platform-compatible (SDP-H1)

EVALUATION BOARD KIT CONTENTS

- EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ evaluation board

EQUIPMENT NEEDED

- PC running Windows® 10 or higher
- SDP-H1 (EVAL-SDP-CH1Z) controller board
- Low noise, precision signal source (such as the SYS-2700 series)
- Standard USB A to USB mini-B
- Band-pass filter suitable for 18-bit testing (value based on signal frequency)

SOFTWARE NEEDED

- ADAQ23876 or ADAQ23878 ACE plugin
- SDP-H1 driver

GENERAL DESCRIPTION

The EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ evaluation boards (see Figure 1) enable simplified evaluation of the ADAQ23876 and ADAQ23878 15 MSPS, 16-/18-bit, high speed, precision µModule® data acquisition solutions, respectively. The EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ demonstrate the performance of the ADAQ23876 and ADAQ23878 µModules, respectively, and are versatile tools for a variety of applications.

The ADAQ23876 and ADAQ23878 µModules combine multiple common signal processing and conditioning blocks into devices that include a low noise, fully differential analog-to-digital converter (ADC) driver, a stable reference buffer, high resolution, 16-/18-bit, 15 MSPS successive approximation register (SAR) ADCs, and the critical passive components necessary for optimum performance.

The EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ interface with a high speed system demonstration platform (SDP), SDP-H1 (EVAL-SDP-CH1Z), via a 160-pin connector, as shown in Figure 2.

For full details on the ADAQ23876 and ADAQ23878, see the ADAQ23876 and ADAQ23878 data sheets, which must be consulted in conjunction with this user guide when using the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ.

EVALUATION BOARD PHOTOGRAPH

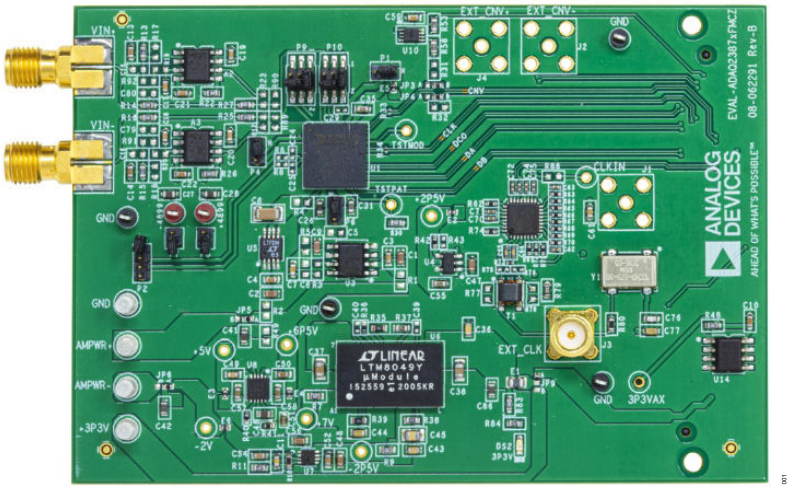

Figure 1.

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

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REVISION HISTORY

1/2022—Rev. 0 to Rev. A

Added EVAL-ADAQ23876FMCZ 1
Changes to User Guide Title 1
Change to Features Section 1
Change to Software Needed Section 1
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Changes to Figure 2 3
Changes to Software Installation Section 7
Changes to Launching the Software Section 9

12/2021—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

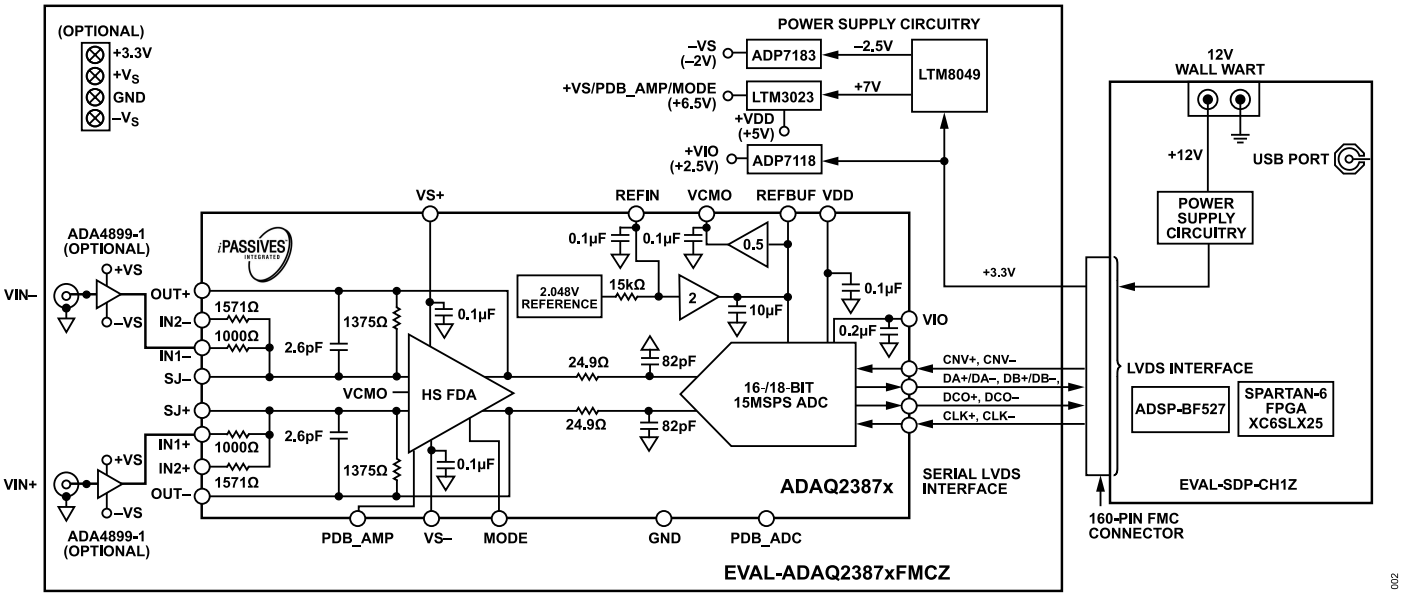

Figure 2. Simplified Evaluation Block Diagram

SETTING UP THE EVALUATION BOARD

Figure 2 shows the simplified evaluation board block diagram of the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ connected to the SDP-H1 controller board. The board consists of one µModule (U1, ADAQ23878 or ADAQ23876), a choice of a 4.096 V reference (U5, LTC6655) or 2.048V reference (U3, ADR4520), on-board power supplies to drive the necessary supply rails using the LTM8049 (U6), the ADP7118 (U4), the ADP7183 (U7), the LT3023 (U8), and an 800 MHz clock distribution IC (U13). The user also has an option to use the A2 and A3 amplifiers, such as the ADA4899-1, when evaluating the ADAQ23876 or ADAQ23878.

SDP-H1 CONTROLLER BOARD

The EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ use a serial peripheral interface (SPI) and connect to the high speed SDP-H1. The SDP-H1 requires power from a 12 V wall adapter. The SDP-H1 has a Xilinx® Spartan 6 and an ADSP-BF527 processor with connectivity to the PC through a USB 2.0 high speed port. The controller boards allow the configuration and capture of data on the daughter boards from the PC via a USB.

The SDP-H1 has a field programmable gate array (FPGA) mezzanine card (FMC) low pin count (LPC) connector with full differential low voltage differential signaling (LVDS) and singled-ended low voltage complementary metal-oxide semiconductor (LVCMOS) support. The SDP-H1 also features the 160-pin connector, found on the SDP-B, which exposes the Blackfin® processor peripherals. This connector provides a configurable serial, parallel I^2C and SPI, and general-purpose input/output (GPIO) communications lines to the attached daughter board for the functional description of the on-board power supplies.

POWER SUPPLIES

By default, all necessary supply rails on the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ are powered by a 3.3 V rail coming from the SDP-H1. The EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ can be powered from an external 3.3 V supply applied using the JP9 solder link if desired (see Table 2). The positive rails of the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ, 7 V (+VS), 5 V (VDD), and 2.5 V (VIO), are generated from a combination of the power µModule, LTM8049 (U6), ADP7118 (U4), and a dual output low dropout (LDO) regulator, LT3023 (U8). The negative rail of the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ, −2.0 V (−VS), is generated by a combination of the power µModule, LTM8049 (U6), and ADP7183 (U7). Each supply rail has necessary decoupling capacitors placed close to the device. A single ground plane is used on the board to minimize the effect of high frequency noise interference.

Table 1. On-Board Power Supplies

Power Supply (V)	Function
+7.5, −2.5	Supply rails using the LTM8049
+7 (default)	VS+ rail using the LT3023
−2 (default)	VS− rail using the ADP7183
+2.5	VIO rail using the ADP7118
+5	VDD rail using LT3023

ANALOG INPUTS

The Subminiature Version A (SMA) connectors (VIN+ and VIN−) on the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ are used to provide analog inputs from a low noise, audio precision signal source (such as the SYS-2700 or the SYS-x555 series). There are two options available to feed analog inputs directly to the ADA4899-1 and ADAQ23876 or ADAQ23878, as shown in Figure

EVALUATION BOARD HARDWARE

25. The optional amplifiers, ADA4899-1 (A2, A3), can be set up in a unity-gain configuration driving the ADAQ23876 or ADAQ23878. In a default configuration of the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ, an input signal via VIN+ and VIN can be fed directly to the ADAQ23876 or ADAQ23878, respectively, by bypassing A2 and A3.

The EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ are factory configured to provide the appropriate input signal type, single-ended or fully differential, and different gain/attenuation or input range scaling. Table 2 lists the necessary jumper positions and link options for different configurations. The default board configuration presents a 4.096 V on the REFBUF pin and a buffered 2.048 V (midscale) of the fully differential ADC driver amplifier (FDA)'s VCMO pin of the ADAQ23876 and ADAQ23878.

To evaluate dynamic performance, a fast Fourier transform (FFT), integral nonlinearity (INL), differential nonlinearity (DNL), or time domain (waveform or histogram) test can be performed by applying a very low distortion ac source. For low input frequency testing below 100 kHz, it is recommended to use a low noise, audio precision signal source (such as the SYS-2700 series) with the outputs set to balanced floating. A different precision signal source can be used alternatively with additional band-pass filtering. The filter bandwidth depends on input bandwidth of interest.

LINK CONFIGURATION OPTIONS

Multiple link options must be set correctly for the appropriate operating setup before applying the power and signal to the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ. Table 2 shows the default positions of the links for the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ.

Table 2. Link Options for the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ

Link	Default	Function	Comment
JP3	Center to B	FPGA CNV+	Change center to A when using ADC_PLL_CNV+.
JP4	Center to B	FPGA CNV-	Change center to A when using ADC_PLL_CNV−.
JP5	Center to A	AMP+	Change center to B when using an external supply.
JP6	Center to A	AMP−	Change center to B when an using external supply. If configured to the single-supply VS− to GND, remove both jumpers (JP6) and install R49 (0 Ω).
JP9	Center to A	3.3 V	Change center to B when using an external 3.3 V supply.
P1	Tie Pin 2 and Pin 3 (connected to GND)	Two-lane digital output modes	Digital input that enables two-lane output mode. Use this jumper to select either single lane or two-lane data output mode. The default setting is Pin 2 and Pin 3. The Pin 2 and Pin 3 setting clocks out all data on the DA± pin. The Pin 1 and Pin 2 setting clocks out data alternately on the DA± and DB± pins.
P2	No connect	ADCIN−	Negative input of an internal ADC. Extra capacitance can be added on this pin to reduce the RC filter bandwidth. Optional for the ADAQ23876 and ADAQ23878.
P3	No connect	ADCIN+	Positive input of an internal ADC. Additional capacitance can be added on this pin to reduce the RC filter bandwidth. Optional for the ADAQ23876 and ADAQ23878.
P4	Tie Pin 1 and Pin 2	PDB_AMP	Active low. Connect this pin to GND to power down the fully differential ADC driver. Otherwise, connect it to VS+.
P5	Not applicable	SDP-H1 FMC connector	The EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ interface to the SDP-H1 via a 160-pin connector.
P6	Tie Pin 1 and Pin 2	PDB_ADC	Digital input that enables the power-down mode. When PDB_ADC is low, an internal ADC core enters power-down mode, and all circuitry (including the LVDS interface) shuts down. When PDB_ADC is high, the device operates normally. Logic levels are determined by VIO.
P7	0 Ω installed	−VS for the ADA4899-1 (A2, A3)	Remove 0 Ω to use the external supply for the ADA4899-1 (A2, A3).
P8	0 Ω installed	+VS for the ADA4899-1 (A2, A3)	Remove 0 Ω to use the external supply for the ADA4899-1 (A2, A3).
P9	Tie Pin 1 and Pin 2, tie Pin 5 and Pin 6	INx−	Gain pin select. Refer to Table 3 for the different gain configurations.
P10	Tie Pin 1 and Pin 2, tie Pin 5 and Pin 6	INx+	Gain pin select. Refer to Table 3 for the different gain configurations.

EVALUATION BOARD HARDWARE

EVALUATION BOARD CONNECTORS

The functional descriptions for all the connectors (including a 160-pin FMC connector used to interface with the SDP-H1) used on the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ are listed in Table 4 and Table 5). There are several test points and single in line (SIL) headers on the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ. These test points provide easy access to on-board signals for troubleshooting and evaluation purposes. Table 3 details the different gain positions for the links of the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ.

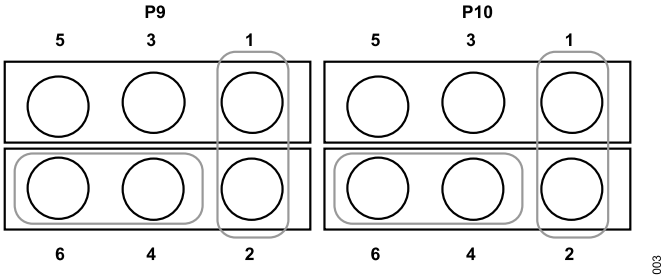

Figure 3. Gain = 0.37

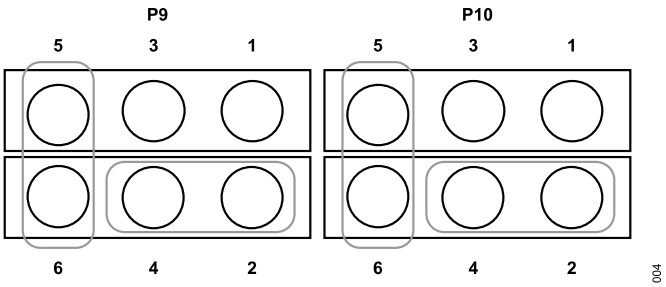

Figure 4. Gain = 0.73

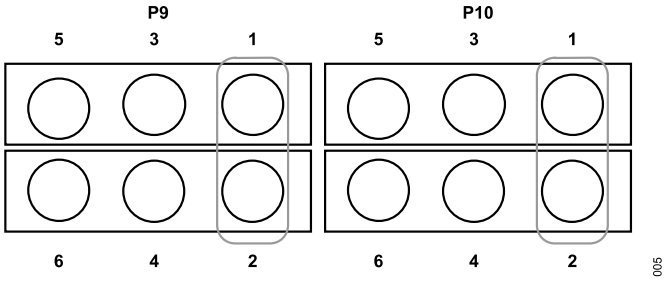

Figure 5. Gain = 0.87

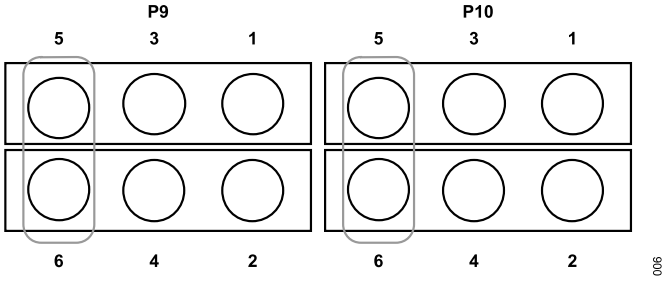

Figure 6. Gain = 1.38

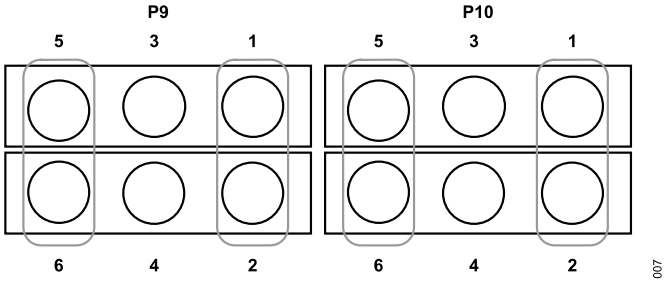

Figure 7. Gain = 2.25

Table 3. Gain Input Configuration

Gain	Input Range (V)	Input Signal on Pins	Test Conditions
0.37	±10	IN2+ IN2−	Connect the OUT+, IN1−, OUT−, and IN1+ pins together (see Figure 3)
0.73	±5	IN1+, IN1−	Connect the OUT+, IN2−, OUT−, and IN2+ pins together (see Figure 4)
0.87	±4.096	IN2+, IN2−	Leave the IN1+ and IN1− pins floating (see Figure 5)
1.38	±2.5	IN1+, IN1−	Leave the IN2+ and IN2− pins floating (see Figure 6)
2.25	±1.5	IN2+/IN1+, IN2−/IN1−	Connect the IN2−, IN1−, IN2+, and IN1+ pins together (see Figure 7)

Table 4. On-Board Connectors

Connector	Function
J1	CLKIN input
J2	EXT_CNV−
J3	External CLK input
J4	EXT_CNV+
VIN+	Analog input V+
VIN−	Analog input V−
+3P3V	External power supply
P5	SDP-H1 FMC connector

EVALUATION BOARD HARDWARE

Table 5. 160-Pin FMC Connector (P5) Details

Signals	Function
OSC_CLK+	100 MHz low jitter positive line of differential pair for carrying clock signals from the daughter board.
OSC_CLK−	100 MHz low jitter negative line of differential pair for carrying clock signals from the daughter board.
CLK±	µModule CLK input signals connected to FPGA Bank 2.[1, 2]
CLK−	µModule CLK input signals connected to FPGA Bank 2.[1, 2]
DCO+	Positive line of differential pair for carrying clock signals from the daughter board.
DCO−	Negative line of differential pair for carrying clock signals from the daughter board.
FPGA_CNV+	User defined signals connected to FPGA Bank 2.[1, 2]
FPGA_CNV−	User defined signals connected to FPGA Bank 2.[1, 2]
DA±	User defined signals connected to FPGA Bank 2.[1]
DB±	User defined signals connected to FPGA Bank 2.[1]
+3P3V_FMC	3.3 V (3 A) power supply to the daughter board.
SCL	I^2C clock line for reading FMC electronically erasable programmable read-only memory (EEPROM).
SDA	I^2C data line for reading FMC EEPROM.
GA0	I^2C Geographical Address 0. Must be connected to Address Pin A1 of the FMC EEPROM.
GA1	I^2C Geographical Address 1. Must be connected to Address Pin A0 of the FMC EEPROM.
3P3VAUX	3.3 V (20 mA) power supply for powering only the FMC EEPROM.
PG_C2M	Active high signal indicating that the 12P0V, 3P3V, and VADJ power supplies are turned on.
CNV_EN	User defined signals connected to FPGA Bank 2.[1]

[1] User defined signals with a P suffix can be used as the positive pin of the differential pair. User defined signals with an N suffix can be used as the negative pin of the differential pair. For further information, see the VITA 57 specification.

[2] User defined signals with a CC suffix are the preferred signal lines on which to transmit clock signals from the controller board to the daughter board. These signal lines are connected to global clock lines on the FPGA, but they can also be used to carry any other user defined signal. For further information, see the VITA 57 specification.

SOFTWARE INSTALLATION

Before using the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ, download and install the Analysis, Control, Evaluation (ACE) software from the ACE software page. Download the ADAQ23876 or ADAQ23878 ACE plugin from the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ product page, respectively, or from the plugin manager in ACE.

ACE is a desktop software application allowing the evaluation and control of multiple evaluation systems across the Analog Devices, Inc., product portfolio. The installation process consists of the ACE software installation and the SDP-H1 driver installation.

To ensure that the evaluation system is properly recognized when it is connected to the PC, install the ACE software and the SDP-H1 driver before connecting the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ and the SDP-H1 to the USB port of the PC.

INSTALLING THE ACE SOFTWARE

To install the ACE software, take the following steps:

1. Download the ACE software to a Windows-based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the software is saved to the following location: **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
4. In the **ACE Setup** window, click **Next >** to continue the installation, as shown in Figure 8.

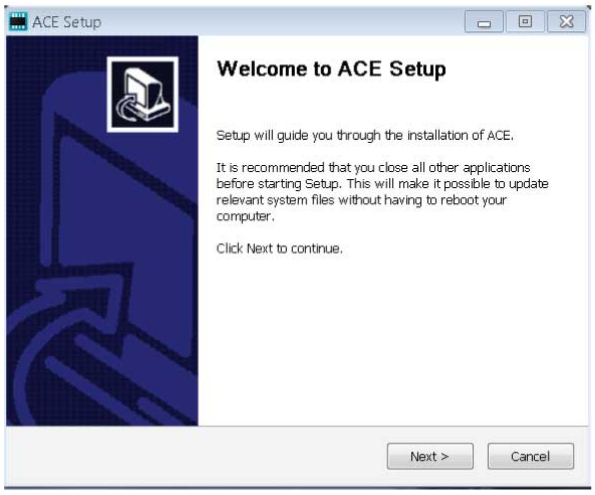

Figure 8. Evaluation Software Install Confirmation

5. Read the software license agreement and click **I Agree** (see Figure 9).

Figure 9. License Agreement

6. Click **Browse...** to choose the installation location and then click **Next** (see Figure 10).

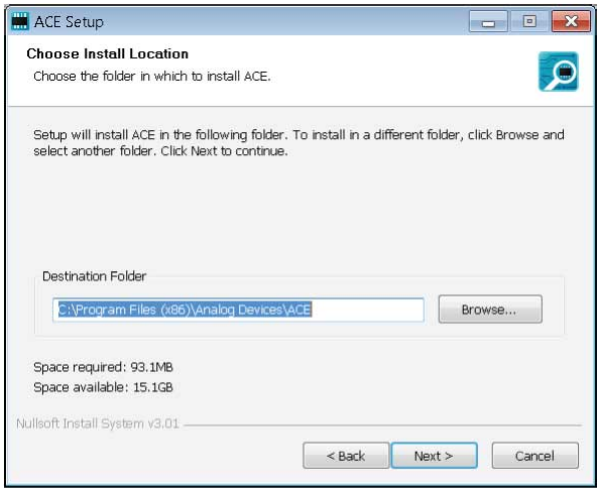

Figure 10. Choose Installation Location

7. Select the **PreRequisites** checkbox to include the installation of the SDP-H1 driver. Click **Install** (see Figure 11).

SOFTWARE INSTALLATION

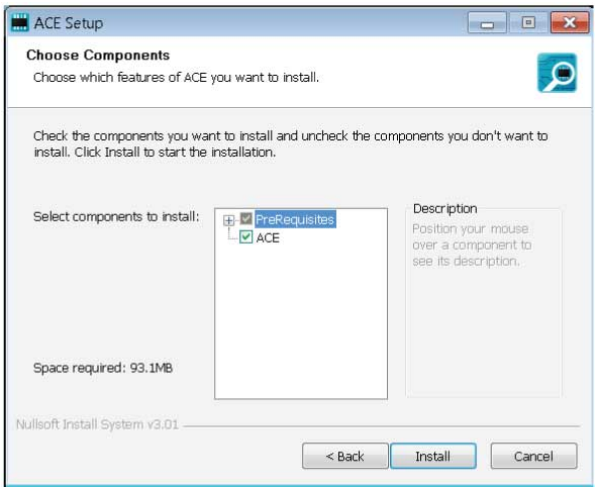

Figure 11. Choose Components

8. The **Windows Security** window opens (see Figure 12). Click **Install**. The installation is in progress. No action is required (see Figure 13).

Figure 12. Windows Security Window

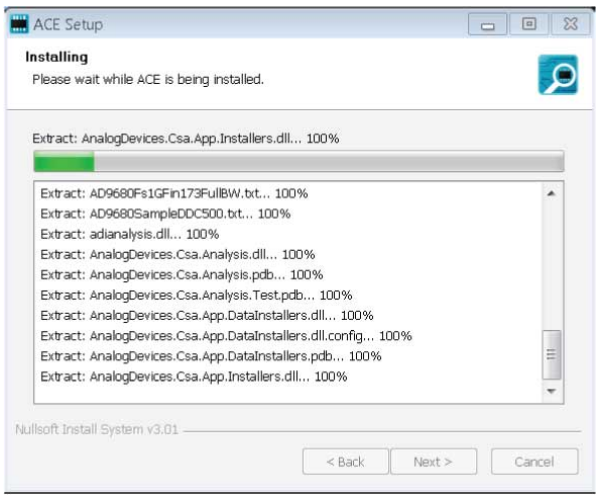

Figure 13. Installation in Progress

9. When the installation is complete, click **Next >** (see Figure 14), and then click **Finish** to complete the installation process.

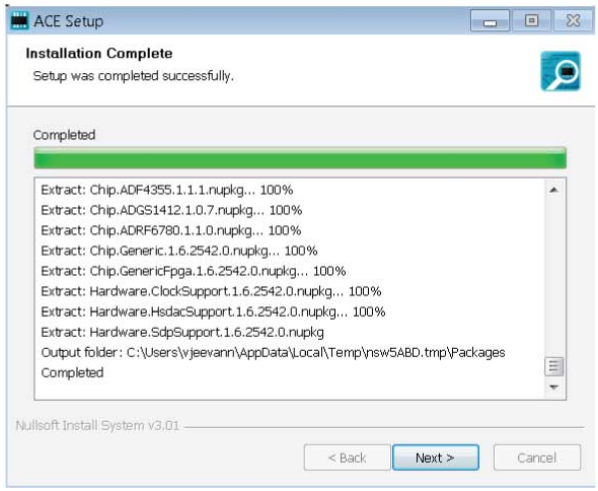

Figure 14. Installation Complete

SOFTWARE OPERATION

LAUNCHING THE SOFTWARE

When the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ and SDP-H1 are properly connected to the PC, launch the ACE software by taking the following steps:

1. From the **Start** menu, select **All Programs** > **Analog Devices** > **ACE** > **ACE.exe** to open the ACE software main shown in Figure 15. The **ADAQ23876 Board** or **ADAQ23878 Board** icon appears in the **Attached Hardware** section, depending on which evaluation board is connected. Note that Figure 15 through Figure 23 show the ACE software with the EVAL-ADAQ23878FMCZ connected.
2. If the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ is not connected to the USB port via the SDP-H1 when the software is launched, the **ADAQ23876 Board** or **ADAQ23878 Board** icon does not appear in the **Attached Hardware** section. Connect the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ and SDP-H1 to the USB port of the PC and wait a few seconds, then continue following these instructions.
3. Double click the **ADAQ23876 Board** or **ADAQ23878 Board** icon to open the board view window.
4. Double click the **ADAQ23876** or **ADAQ23878** chip icon in the board view window to open the chip view window shown in Figure 16.
5. Click **Software Defaults** and then click **Apply Changes** to apply the default settings to the ADAQ23876 or ADAQ23878.
6. Click **Proceed to Analysis** in the chip view window to open the analysis view window shown in Figure 17.

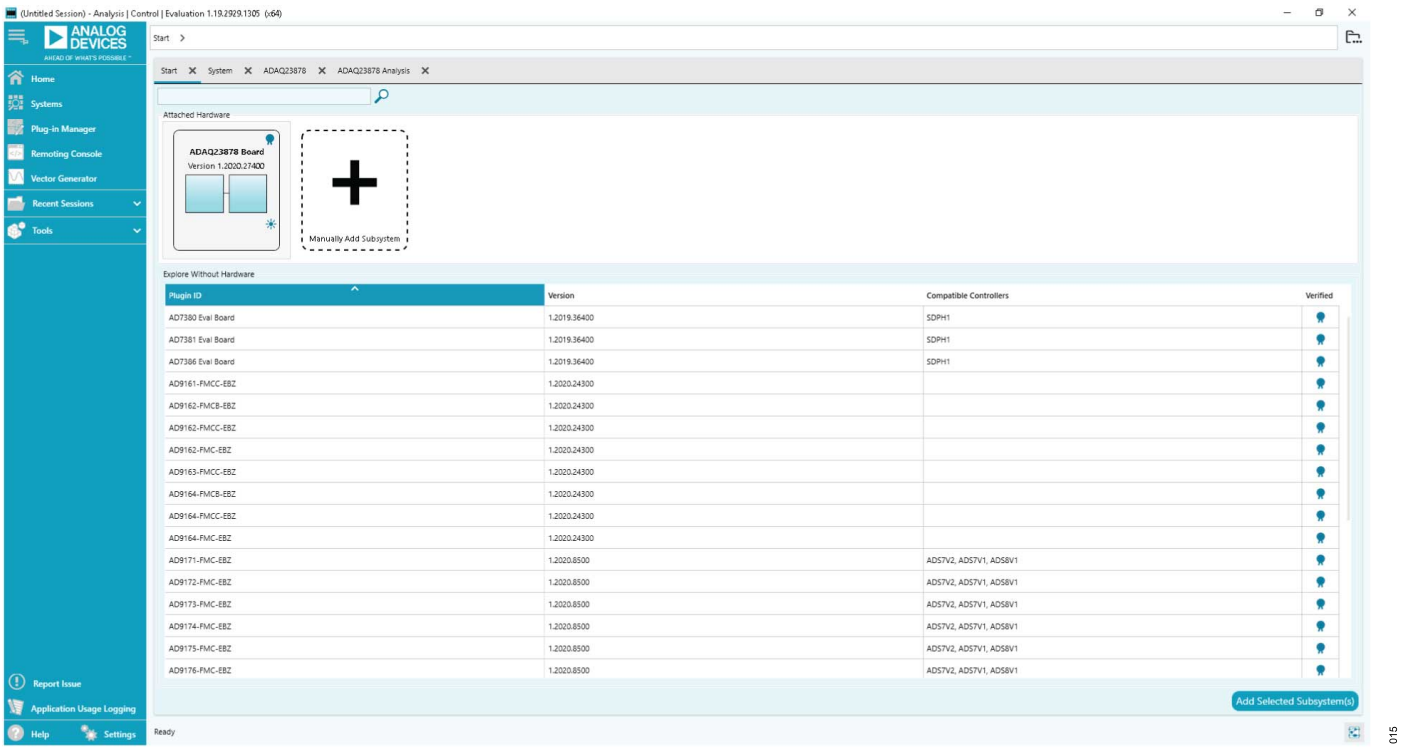

Figure 15. ACE Software Main Window

SOFTWARE OPERATION

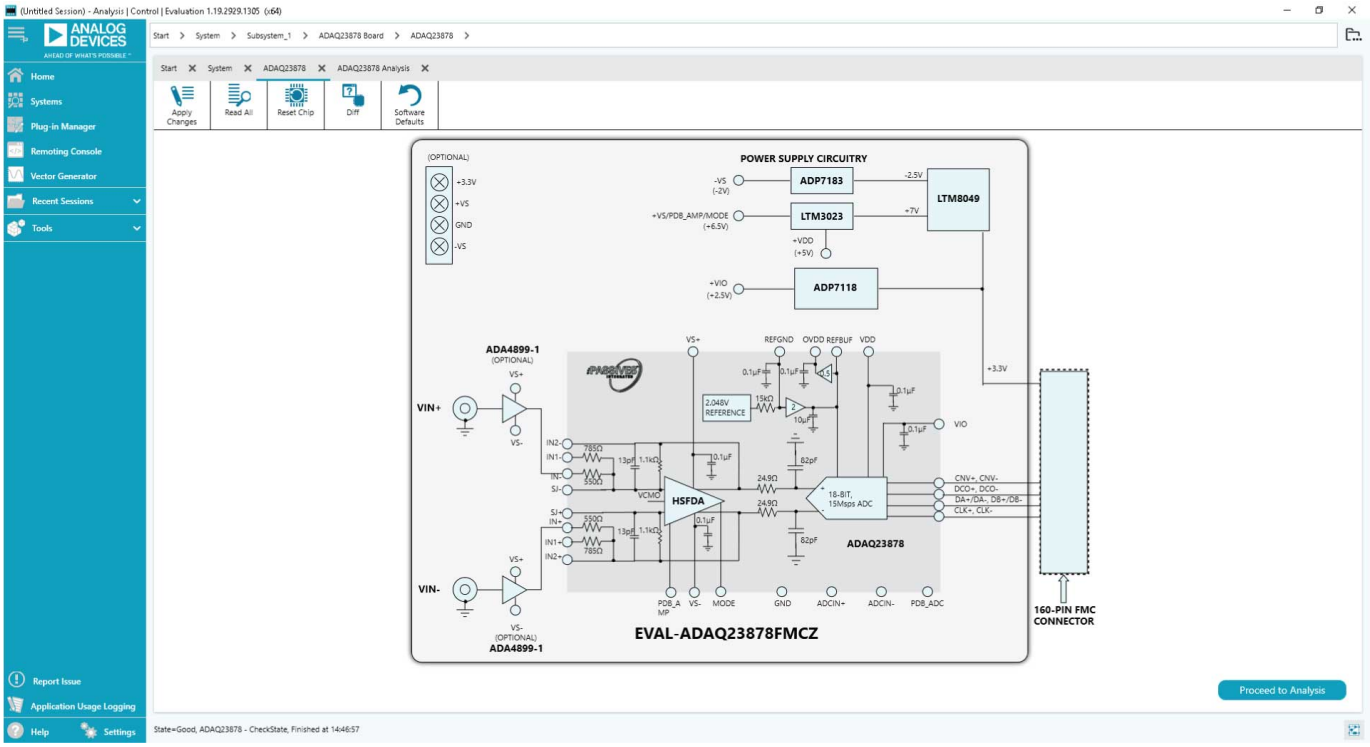

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Figure 16. Chip View

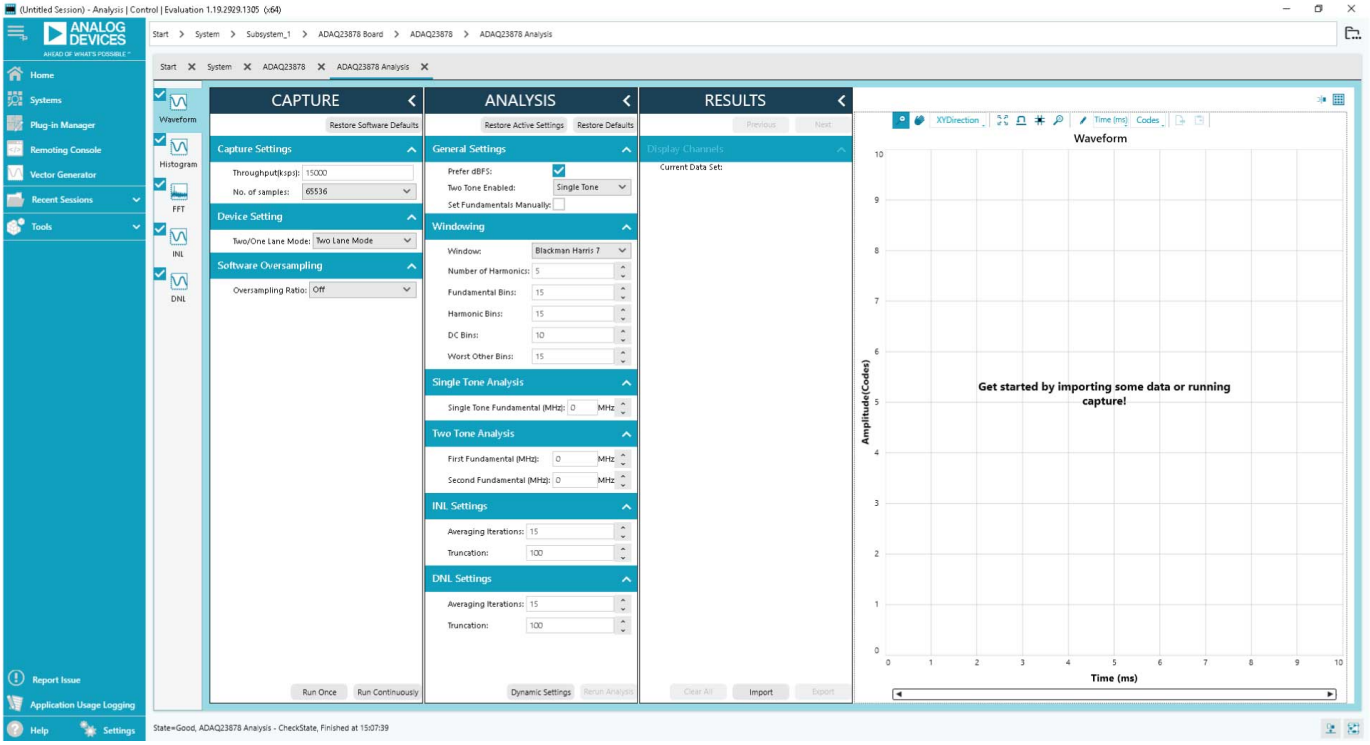

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Figure 17. Analysis View

SOFTWARE OPERATION

EXITING THE SOFTWARE

To exit the ACE software, click the file icon on the upper right tab and then click **Exit**.

DESCRIPTION OF ANALYSIS WINDOW

Click **Proceed to Analysis** in the chip view window to open the analysis view window shown in Figure 17. The analysis view window contains the **Waveform** tab, **Histogram** tab, **FFT** tab, **INL** tab, and **DNL** tab.

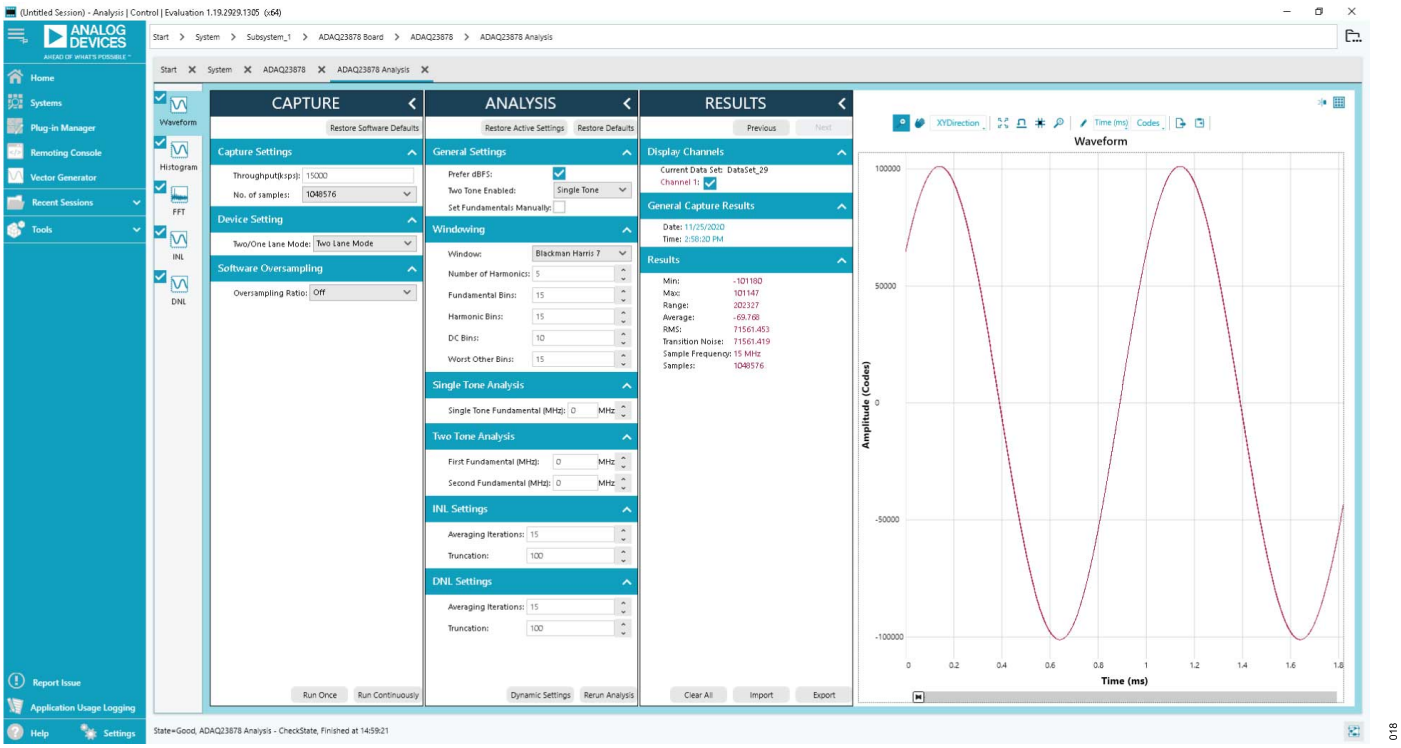

Figure 18. Waveform Tab

SOFTWARE OPERATION

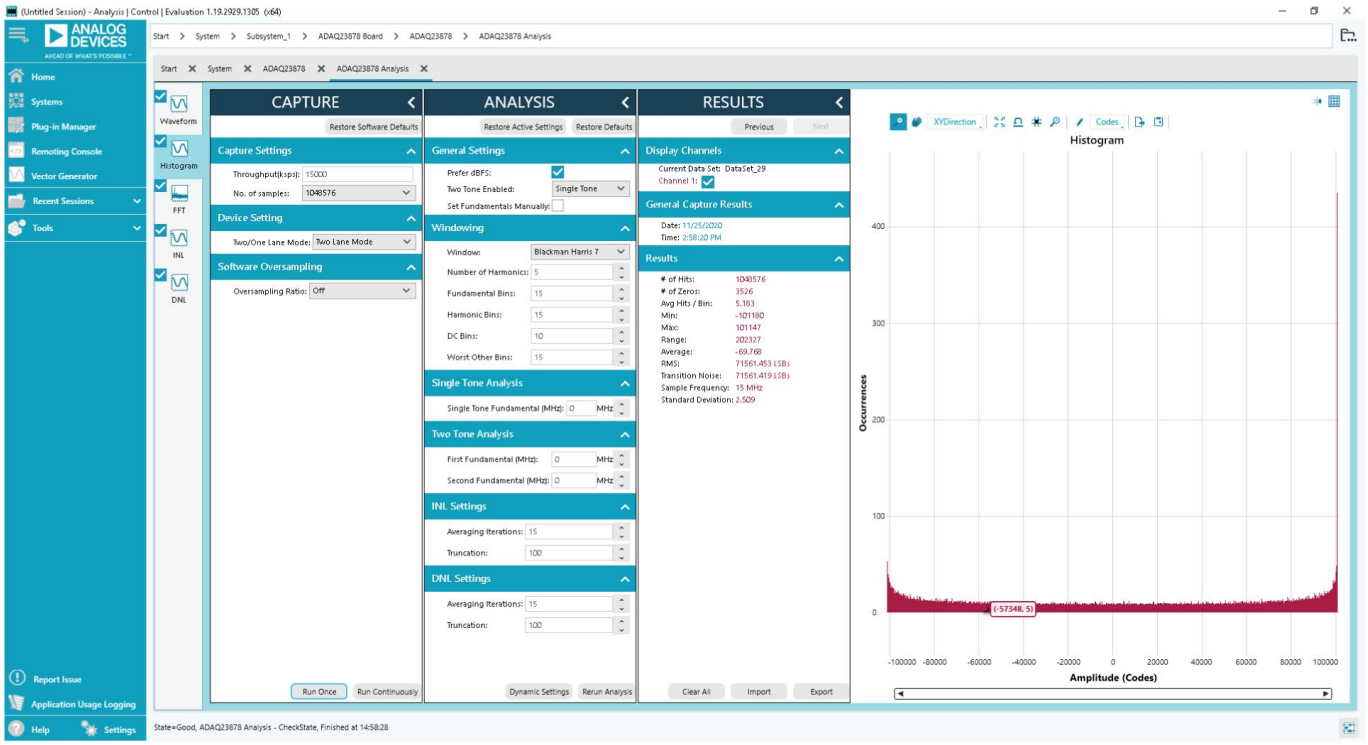

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Figure 19. Histogram Tab

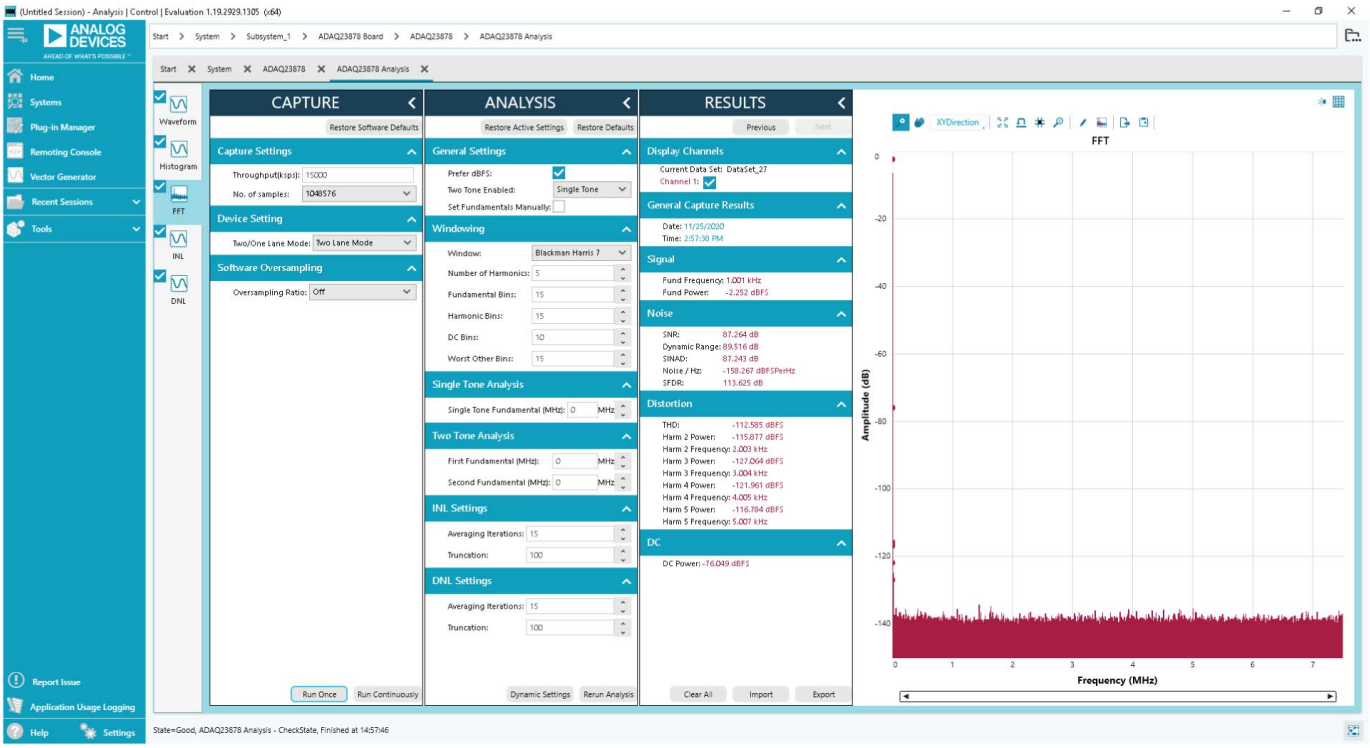

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Figure 20. FFT Tab

SOFTWARE OPERATION

Waveform Tab

The **Waveform** tab displays results in the time domain, as shown in Figure 18.

CAPTURE Pane

The **Capture** pane contains the capture settings, which reflect onto the registers automatically before data capture.

The **Sample Count** pulldown menu in the **General Capture Settings** section allows the user to select the number of samples per channel per capture.

The user can enter the input sample frequency in kSPS in the **Throughput(ksps)** field in the **General Capture Settings** section. Refer to the ADAQ23876 or ADAQ23878 data sheet to determine the maximum sampling frequency for the selected mode.

Click **Run Once** in the **Device Settings** section to start a data capture of the samples at the sample rate specified in the **Sample Count** pulldown menu. These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Click **Run Continuously** in the **Device Settings** section to start a data capture that gathers samples continuously with one batch of data at a time.

RESULTS Pane

The **Display Channels** section allows the user to select which channels to capture. The data for a specific channel is only shown if that channel is selected before the capture.

The **Results** section displays amplitude, sample frequency, and noise analysis data for the selected channels.

Click **Export** to export captured data. The waveform, histogram, and FFT data is stored in .xml files along with the values of parameters at capture.

The data **Waveform** graph shows each successive sample of the µModule output. The user can zoom in on and pan across the **Waveform** graph using the embedded waveform tools. Select the channels to display in the **Display Channels** section.

Select **Codes** above the **Waveform** graph to select whether the graph displays in units of **Codes**, **Hex**, or **Volts**. The axis controls are dynamic.

When selecting either **y-scale dynamic** or **x-scale dynamic**, the corresponding axis width automatically adjusts to show the entire range of the µModule results after each batch of samples. Select the dynamic using the **XYDirection** tool above the **Waveform** graph.

Histogram Tab

The **Histogram** tab contains the **Histogram** graph and the **RESULTS** pane, as shown in Figure 19.

The **RESULTS** pane displays the information related to the dc performance.

The **Histogram** graph displays the number of hits per code within the sampled data. This graph is useful for dc analysis and indicates the noise performance of the device.

FFT Tab

The **FFT** tab displays FFT information for the last batch of samples gathered, as shown in Figure 20. The **FFT** tab also allows the oversampling function with an oversampling rate (OSR) up to 256×, as shown in Figure 21. Oversampling by a factor of four provides one additional bit of resolution, or a 6 dB increase in the dynamic range (DR) of the ADAQ23876 or ADAQ23878. In other words,

$\Delta DR = 10 \times \log10\ (OSR)$ (in dB)

SOFTWARE OPERATION

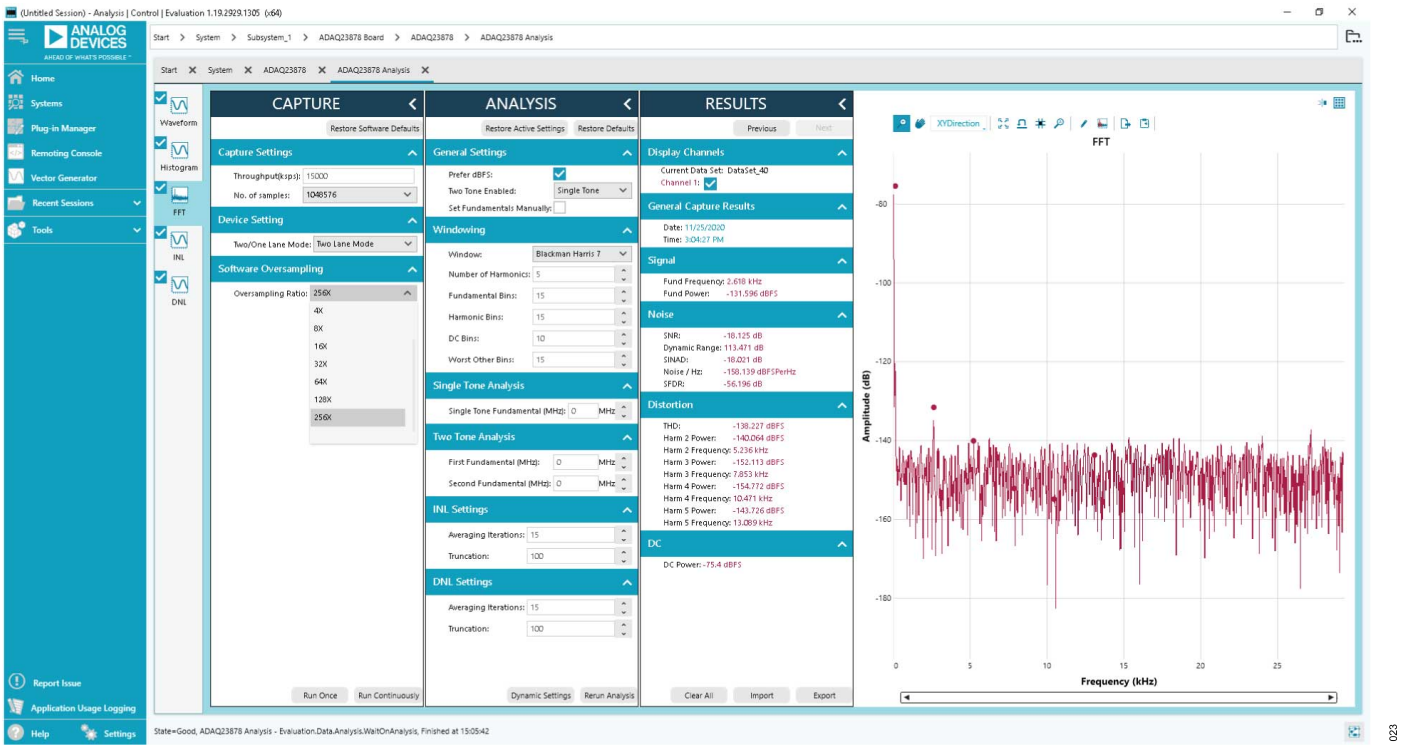

Figure 21. FFT with Oversampling (OSR) of 256×, Inputs Shorted

INL Tab and DNL Tab

The **INL** tab and **DNL** tab display linearity analysis. INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

To perform a linearity test, apply a sinusoidal signal with 0.5 dB above full scale to the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ at the VIN+ and VIN− SMA inputs. Set the number of hits per code and adjust to the desired accuracy. Using a large number of hits per code results in a significant test time. Figure 22 and Figure 23 display captured data that includes the ±INL and ±DNL positions.

SOFTWARE OPERATION

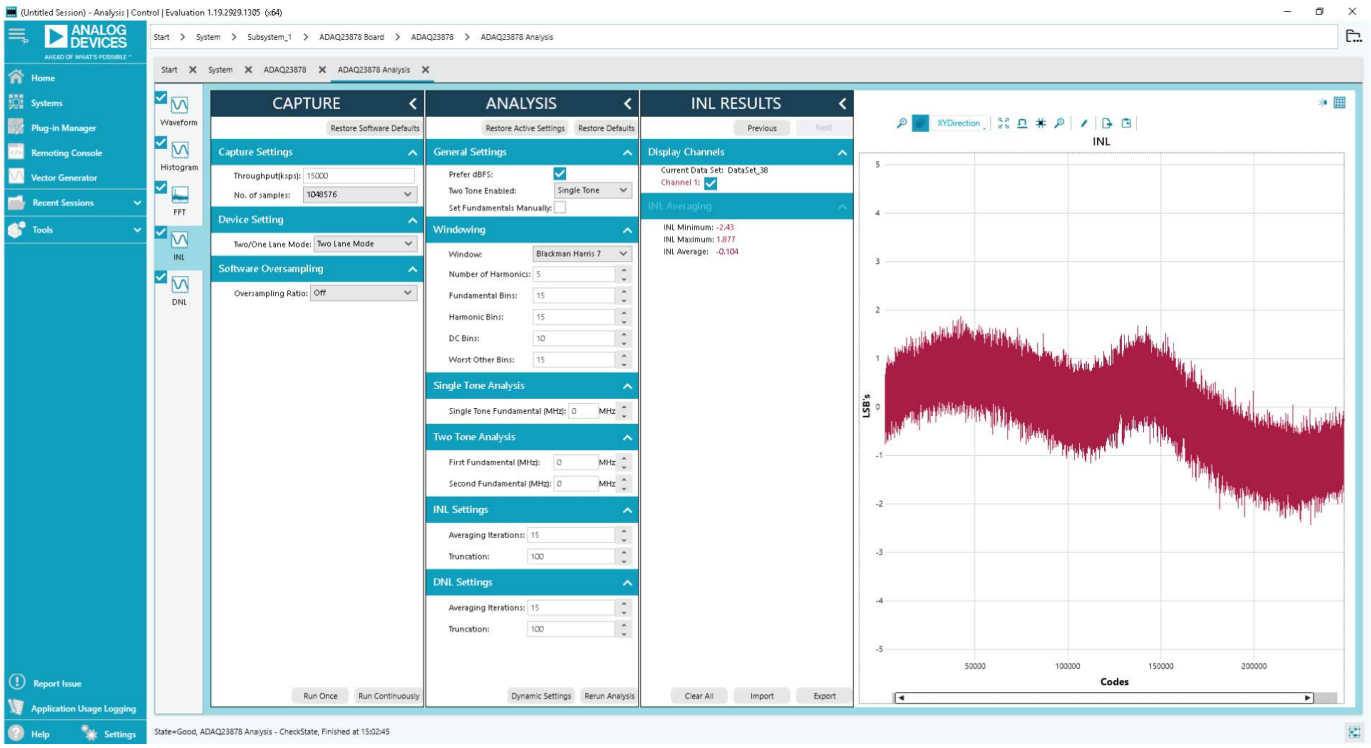

Figure 22. INL Tab

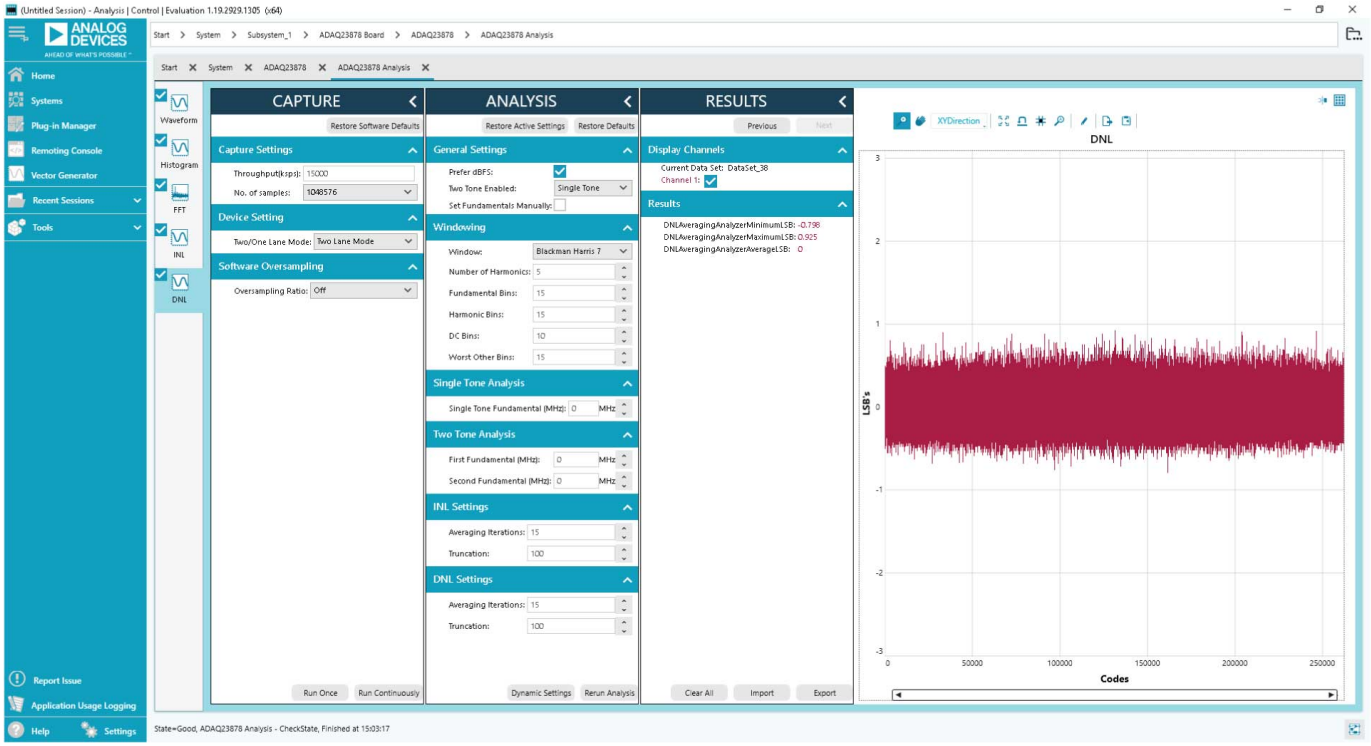

Figure 23. DNL Tab

SOFTWARE OPERATION

ANALYSIS Pane

The **General Settings** section allows the user to set up the preferred configuration of the FFT analysis. This configuration sets how many tones are analyzed and if the fundamental is set manually.

The **Windowing** section allows the user to set up the preferred windowing type to use in the FFT analysis and the number of harmonic bins and fundamental bins that must be included in the analysis.

The **Single Tone Analysis** and the **Two-Tone Analysis** sections sets up the fundamental frequencies included in the FFT analysis. When one frequency is analyzed, use the **Single Tone Analysis** section. When two frequencies are analyzed, use the **Two-Tone Analysis** section.

RESULTS Pane

The **Signal** section displays the sample frequency, fundamental frequency (**Fund Frequency**), and fundamental power (**Fund Power**).

The **Noise** section displays the signal-to-noise ratio (**SNR**) and other noise performance results.

The **Distortion** section displays the harmonic content of the sampled signal and dc power when viewing the FFT analysis.

TROUBLESHOOTING

The SDP-H1 is the communication link between the PC and the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ. Figure 2 shows a diagram of the connections between the EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ and the SDP-H1.

To ensure that the evaluation system is properly recognized when it is connected to the PC, install the ACE software and the SDP-H1 driver before connecting the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ and the SDP-H1 to the USB port of the PC.

When the software installation is complete, set up the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ and the SDP-H1 as described in the Connecting the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ and the SDP-H1 to the PC section and Verifying the Board Connection section.

CONNECTING THE EVAL-ADAQ23876FMCZ OR EVAL-ADAQ23878FMCZ AND THE SDP-H1 TO THE PC

To connect the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ and the SDP-H1 to the PC, take the following steps:

1. Ensure that all configuration links are in the appropriate positions, as described in Table 1.
2. Connect the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ securely to the 160-way connector on the SDP-H1. The EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ do not require an external power supply adapter.
3. Connect the SDP-H1 to the PC via the USB cable enclosed in the SDP-H1 kit. Refer to Figure 2.

VERIFYING THE BOARD CONNECTION

To verify the board connection, take the following steps:

1. Allow the found new hardware wizard to run after the SDP-H1 is plugged in to the PC. If using Windows XP®, search for the SDP-H1 driver. Choose to automatically search for the SDP-H1 driver if prompted by the operating system.
2. A dialog box may open asking for permission to allow the program to make changes to the computer. In this case, click **Yes**. The **Computer Management** window opens.
3. Under **System Tools**, click **Device Manager** and use the **Device Manager** window to ensure that the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ is connected to the PC properly.
4. If the SDP-H1 driver software is installed and the board is connected to the PC properly, **Analog Devices SDP-H1** appears under **ADI Development Tools** in the **Device Manager** window, as shown in Figure 24.

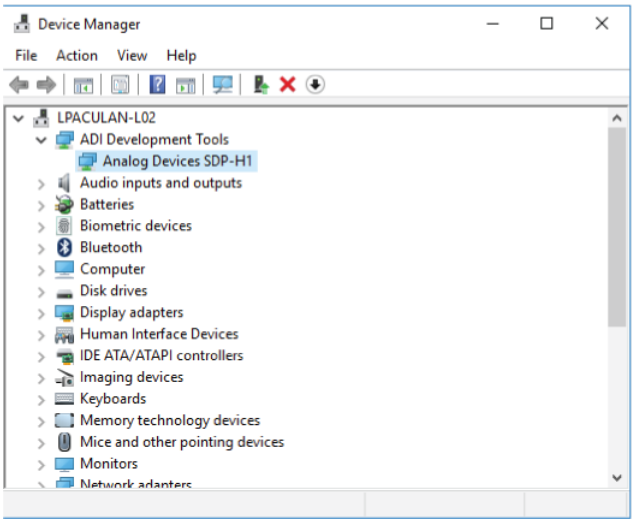

Figure 24. Windows Device Manager

DISCONNECTING THE EVAL-ADAQ23876FMCZ OR EVAL-ADAQ23878FMCZ

Always remove power from the SDP-H1 or press the reset tact switch located along the mini USB port before disconnecting the EVAL-ADAQ23876FMCZ or EVAL-ADAQ23878FMCZ from the SDP-H1.

BOARD LAYOUT GUIDELINES

The printed circuit board (PCB) layout is critical for preserving signal integrity and achieving the expected performance from the ADAQ23876 and ADAQ23878. A multilayer board with an internal, clean ground plane in the first layer beneath the ADAQ23876 and ADAQ23878 is recommended. Care must be taken with the placement of individual components and routing of various signals on the board. It is highly recommended to route input and output signals symmetrically. Solder the ground pins of the ADAQ23876 or ADAQ23878 directly to the ground plane of the PCB using multiple vias. Remove the ground and power planes under the analog input/output and digital input/output (including F1 and F2) pins of the ADAQ23876 or ADAQ23878 to avoid undesired parasitic capacitance. Any undesired parasitic capacitance can impact the distortion and linearity performance of the ADAQ23876 and ADAQ23878.

The pinout of the ADAQ23876 and ADAQ23878 eases the layout and allows its analog signals on the left side and its digital signals on the right side. The sensitive analog and digital sections must be separated on the PCB while keeping the power supply circuitry away from the analog signal path. Fast switching signals, such as CNV± or CLK±, and the DA± and DB± digital outputs must not run near or cross over analog signal paths to prevent noise coupling to the ADAQ23876 and ADAQ23878.

Good quality ceramic bypass capacitors of at least 2.2 µF (0402, X5R) must be placed at the output of LDO regulators generating

TROUBLESHOOTING

the µModule supply rails (VDD, VIO, VS+, and VS−) to GND to minimize electromagnetic interference (EMI) susceptibility and to reduce the effect of glitches on the power supply lines. All the other required bypass capacitors are laid out within the ADAQ23876 and ADAQ23878, saving extra board space and cost. When the external decoupling capacitors on REFIN, VDD, and VIO pins near the µModule are removed, there is no significant performance impact.

MECHANICAL STRESS

The mechanical stress of mounting a device to a board can cause subtle changes to the SNR and internal voltage reference. The best soldering method is to use IR reflow or convection soldering with a controlled temperature profile. Hand soldering with a heat gun or a soldering iron is not recommended.

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

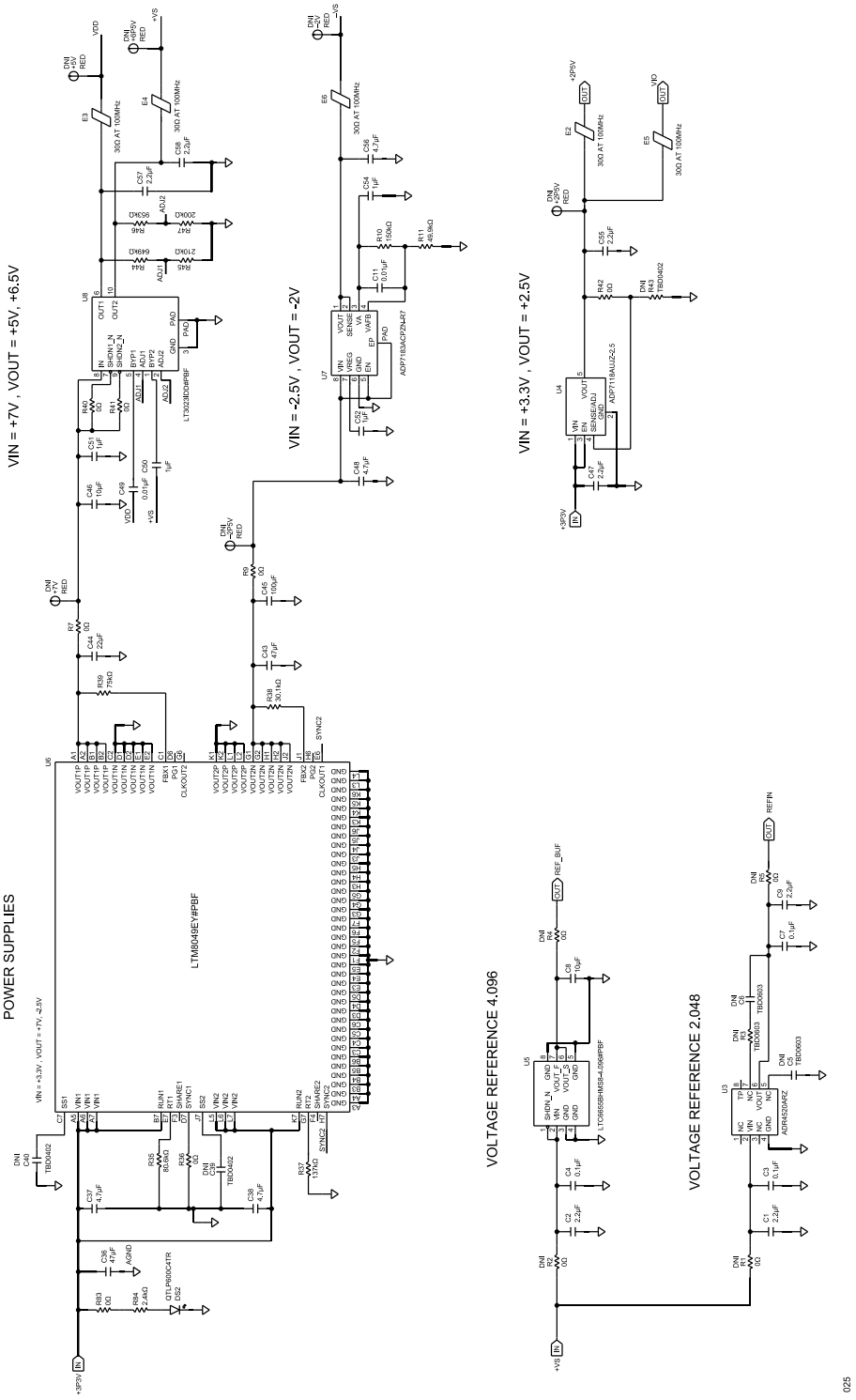

Figure 25. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Schematic, Power Supplies

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

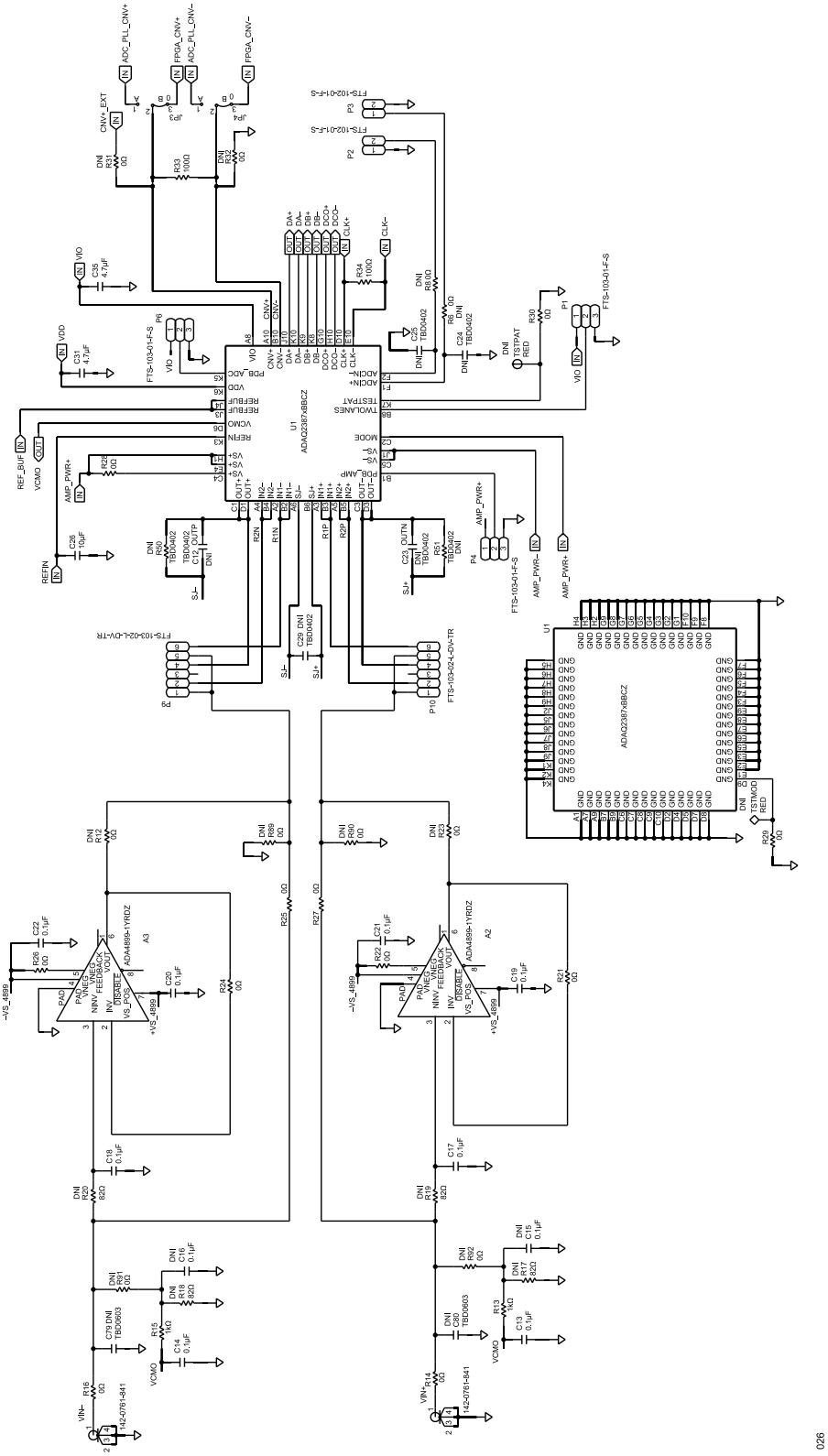

Figure 26. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Schematic, Input Signal Path

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

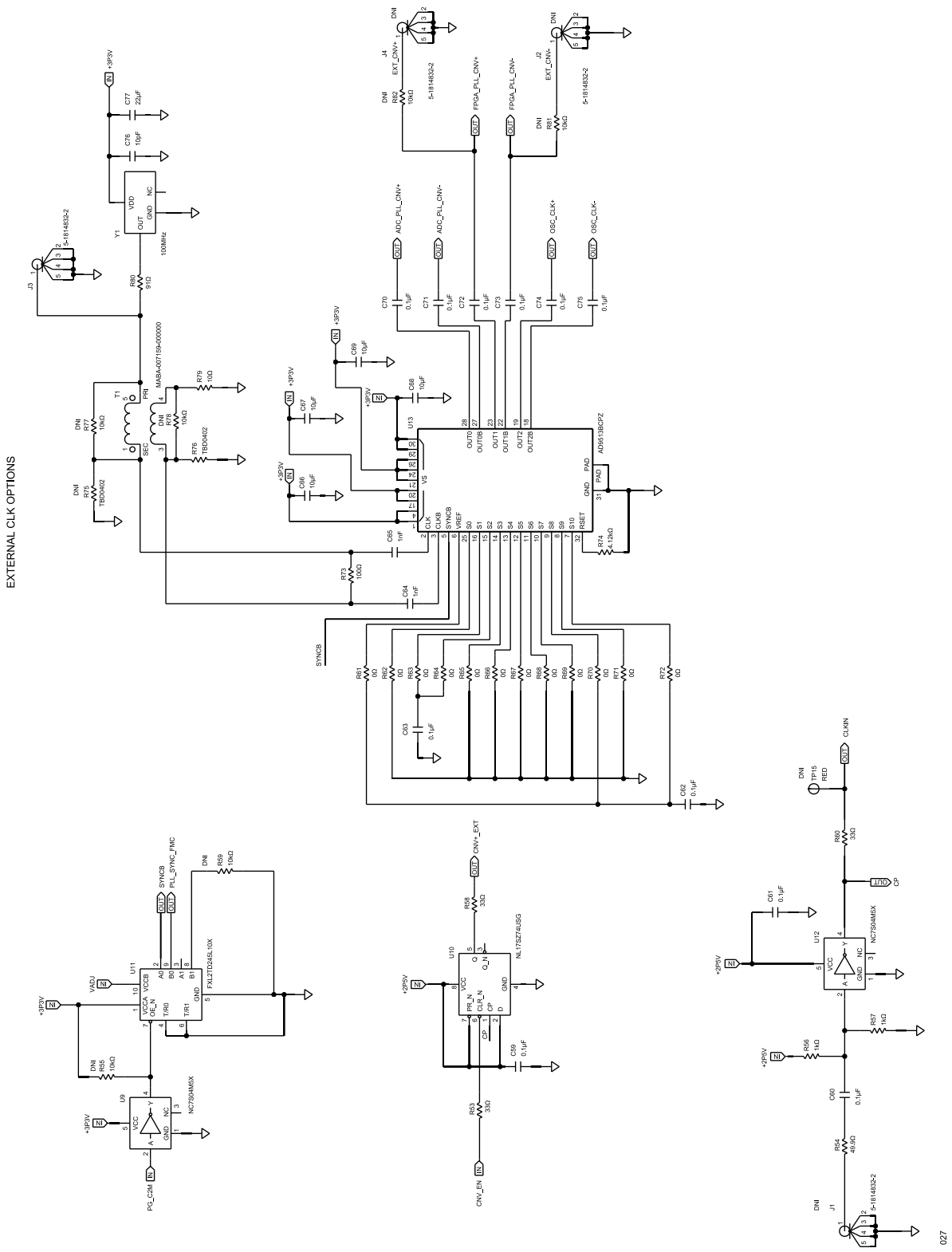

Figure 27. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Schematic, External Clock

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

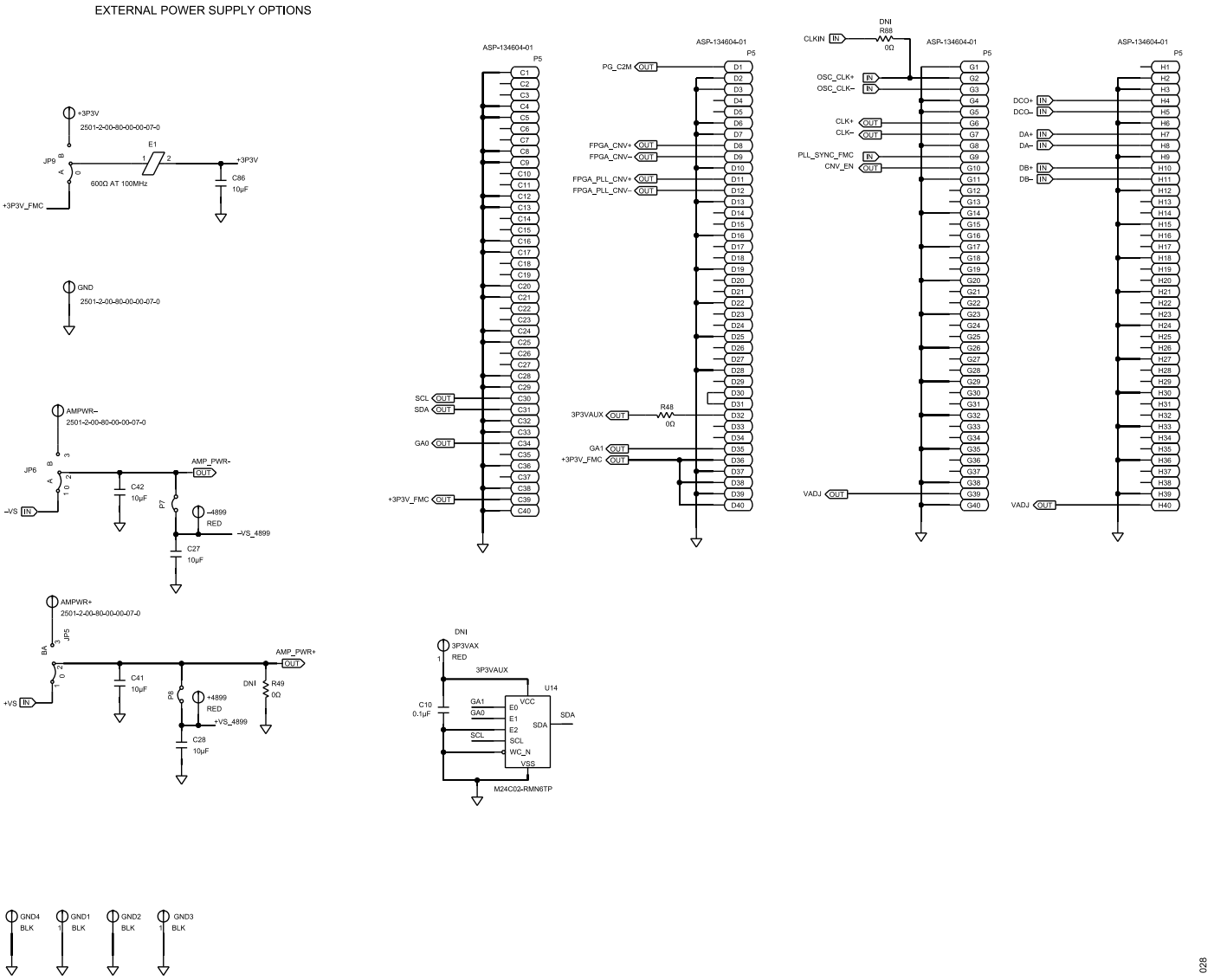

Figure 28. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Schematic, FMC Connector and External Supplies

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

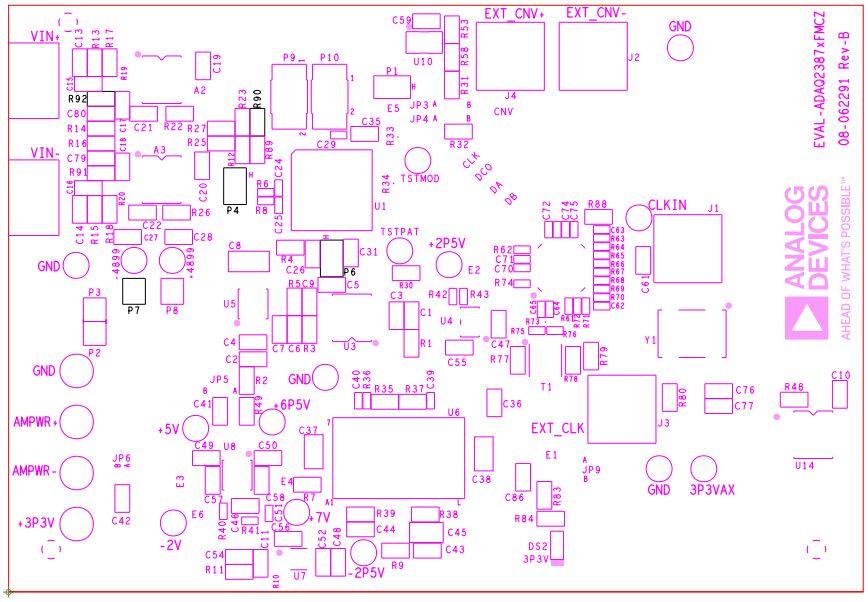

Figure 29. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Primary Silkscreen

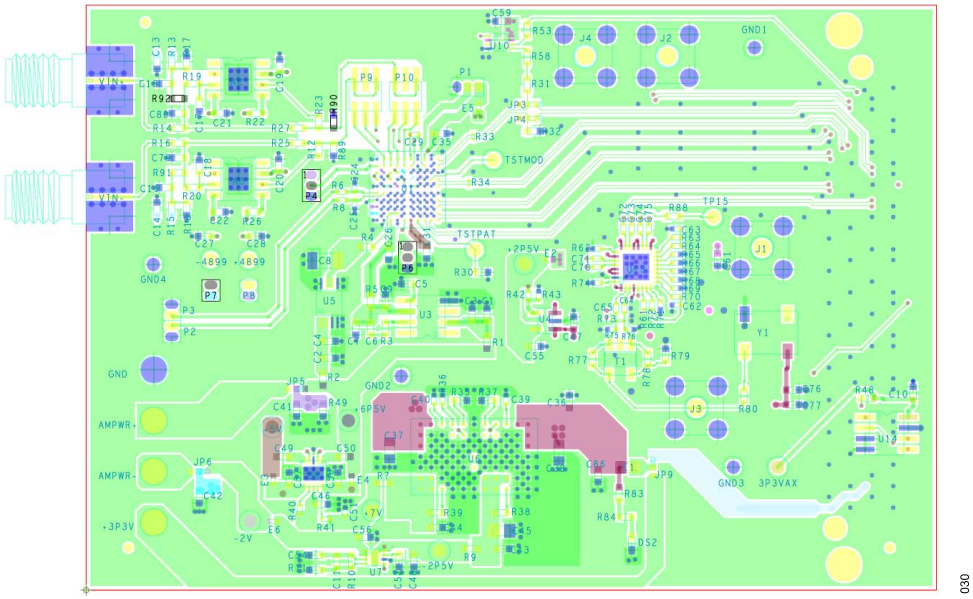

Figure 30. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Primary Layer, L1

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

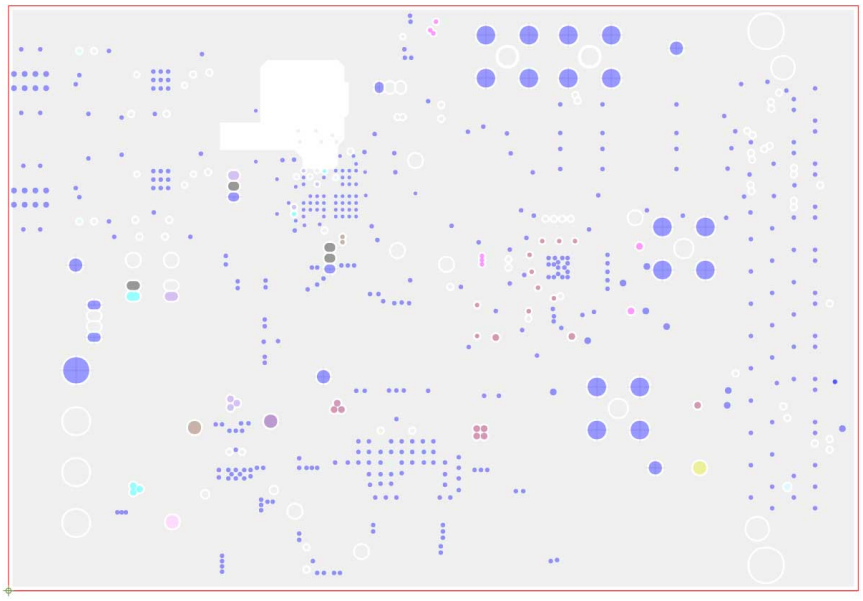

Figure 31. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Ground Layer, L2

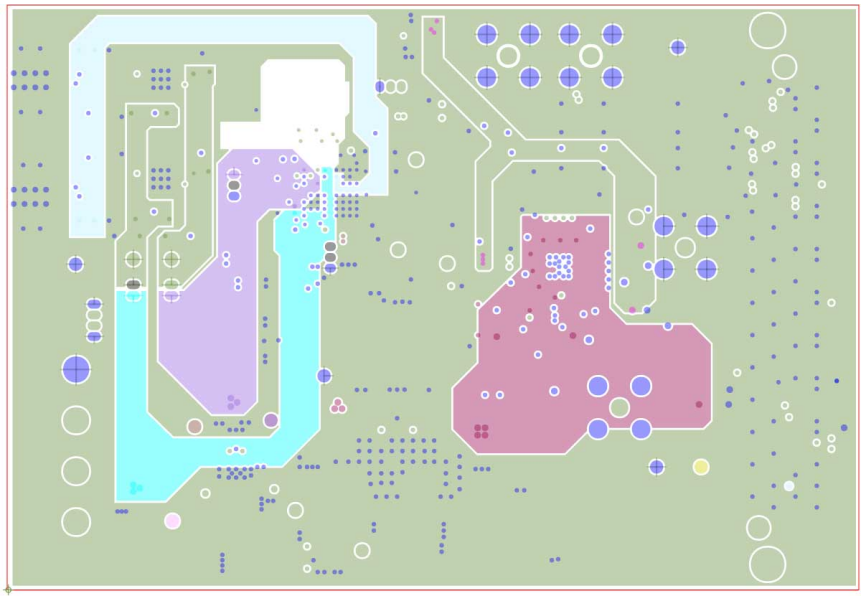

Figure 32. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Power Layer, L3

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

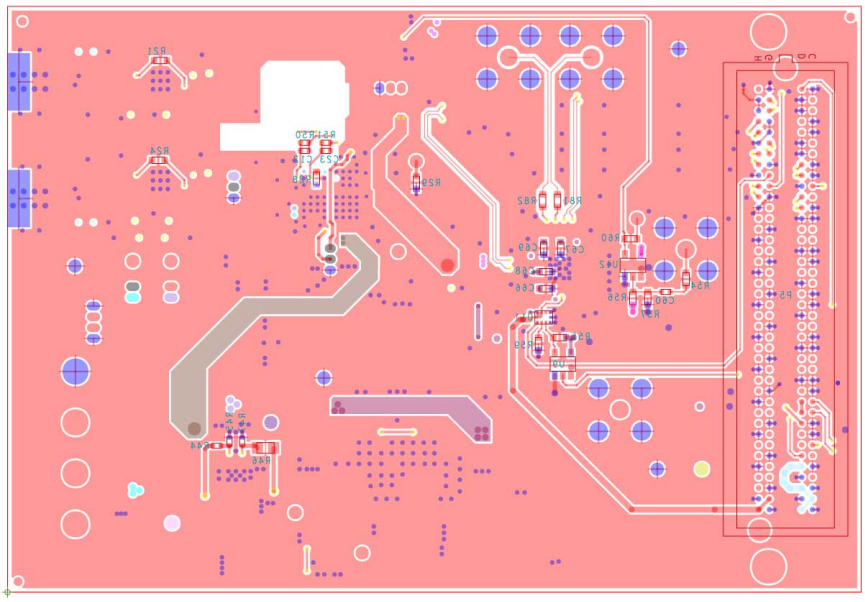

Figure 33. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Bottom Layer, L4

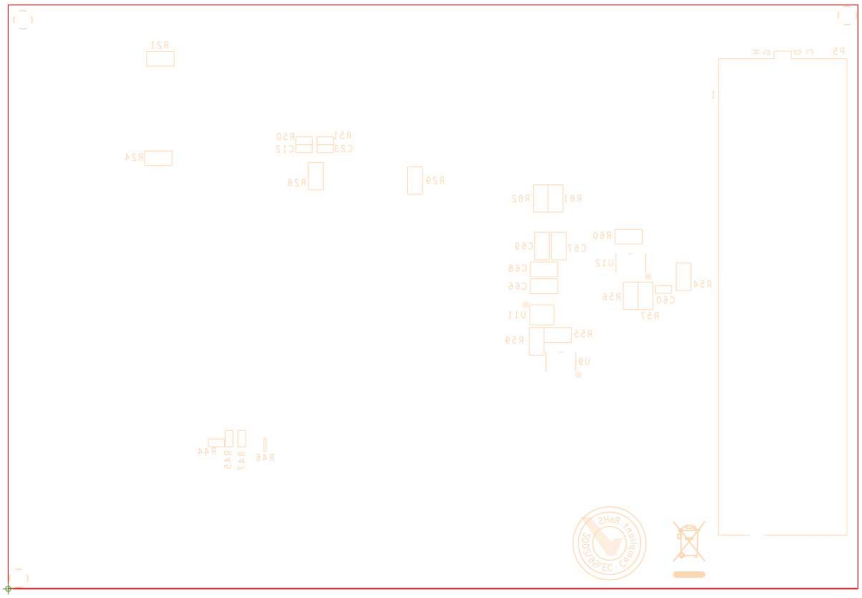

Figure 34. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Secondary Silkscreen

EVALUATION BOARD SCHEMATICS AND SILKSCREENS

Figure 35. EVAL-ADAQ23876FMCZ and EVAL-ADAQ23878FMCZ Board Drill Chart and Size 69 mm × 100.5 mm

ORDERING INFORMATION

Table 6. Bill of Materials

Qty	Reference Designator	Description	Part No.	Manufacturing
4	+3P3V, AMPWR+, AMPWR−, GND	Connector PCB solder terminal turrets	2501-2-00-80-00-00-07-0	Mill-max
2	+4899, −4899	Connector PCB test points, red	5000	Keystone Electronics
2	A2, A3	Unity-gain stable, ultralow distortion	ADA4899-1YRDZ	Analog Devices
4	C1, C2, C9, C47	2.2 µF ceramic capacitors, X5R, general-purpose	GRM188R61H225KE11J	Murata
4	C3, C4, C7, C10	0.1 µF ceramic capacitors, X7R, 0603	06035C104KAT2A	AVX
1	C11	0.01 µF multilayer ceramic capacitor, X7R, automotive grade	C0603C103K5RECAUTO	Kemet
8	C13, C14, C17 to C22	0.1 µF ceramic capacitors, X7R	06035C104J4Z2A	AVX
7	C26, C27, C28, C41, C42, C46, C86	10 µF ceramic capacitors, X5R, general-purpose	GRM188R61E106KA73D	Murata
2	C31, C35	4.7 µF ceramic capacitors, X5R, commercial grade	C0603C475K8PACTU	Kemet
2	C36, C43	47 µF ceramic capacitors, X5R, general-purpose	GRM188R60J476ME15D	Murata
2	C37, C38	4.7 µF ceramic capacitors, multilayer, X5R	CC0805KKX5R8BB475	Yageo
1	C44	22 µF ceramic capacitor, X5R, general-purpose	GRM188R61A226ME15D	Murata
1	C45	100 µF ceramic capacitor, X5R, general-purpose	GRM21BR60J107ME15K	Murata
2	C48, C56	4.7 µF ceramic capacitors, X6S, general-purpose	GRM188C81C475KE11D	Murata
1	C49	0.01 µF ceramic capacitor, chip C0G 0603	C0603C103J3GACTU	Kemet
1	C50	1 µF ceramic capacitor, X7R	0603YC105KAT2A	AVX
1	C51	1 µF ceramic capacitor, X7R, general-purpose	GRM155R70J105KA12D	Murata
2	C52, C54	1 µF ceramic capacitors, X7R	8.85012E+11	Wurth Elektronik
3	C55, C57, C58	2.2 µF ceramic capacitors, X7R, general-purpose	GRM188R71A225KE15D	Murata
2	C59, C61	0.1 µF ceramic capacitors, 0603, X7R	C0603C104K4RAC	Kemet
9	C60, C62, C63, C70 to C75	0.1 µF ceramic capacitors, X7R	C0402C104K4RACTU	Kemet
2	C64, C65	1 nF ceramic capacitors, 5%, 50 V, C0G NP0, 0402	C0402C102J5GACTU	Kemet
4	C66 to C69	10 µF ceramic capacitors, X5R	C1608X5R1A106K080AC	TDK
1	C76	10 pF ceramic capacitor, multilayer, C0G	C1608C0G1H100D080DA	TDK
1	C77	22 µF ceramic capacitor, X5R	C1608X5R0J226M080AC	TDK
1	C8	10 µF ceramic capacitor, X7R	C3216X7R1V106M160AC	TDK
1	DS2	LED green clear	QTLP600C4TR	Fairchild Semiconductor
1	E1	Inductor chip ferrite bead	MPZ2012S601AT000	TDK
5	E2 to E6	Inductor chip ferrite bead	BLM15PD300SN1D	Murata Manufacturing
4	GND1, GND2, GND3, GND4	Connector PCB test points, black	20-2137	Vero Technologies
1	J3	Connector PCB straight SMA die cast	5-1814832-2	TE Connectivity, Ltd.
5	JP3 to JP6, JP9	0 Ω resistor jumpers, surface-mount device (SMD) R0402	ERJ-2GE0R00X	Panasonic
3	P1, P4, P6	Connector PCB, micro low profile term strips	FTS-103-01-F-S	Samtec
2	P9, P10	Connector PCB male header dual row unshrouded, micro low profile term strips, 1.27 mm pitch	FTS-103-02-L-DV-TR	Samtec
4	P2, P3, P7, P8	Connector PCB micro low profile term strips, 1.27 mm pitch	FTS-102-01-F-S	Samtec
1	P5	Connector PCB single-end array male 160-position	ASP-134604-01	Samtec
1	R10	150 kΩ resistor precision thick film chip, R0603	ERJ-3EKF1503V	Panasonic
1	R11	49.9 kΩ resistor precision thick film chip	ERJ-3EKF4992V	Panasonic
2	R13, R15	1 kΩ resistors, thick film chip	MC0063W060311K	Multicomp
15	R7, R9, R14, R16, R21, R22, R24 to R30, R48, R83	0 Ω resistors film SMD, R0603	MC0603WG00000T5E-TC	Multicomp
3	R33, R34, R73	100 Ω resistors, precision thick film chip	ERJ-1GNF1000C	Panasonic
1	R35	80.6 kΩ resistor thick film chip	CRCW060380K6FKEA	Vishay
16	R36, R40, R41, R42, R61 to R72	0 Ω resistors, thick film chip	MC00625W040210R	Multicomp
1	R37	137 kΩ resistor thick film chip	MC0063W06031137K	Multicomp

ORDERING INFORMATION

Table 6. Bill of Materials

Qty	Reference Designator	Description	Part No.	Manufacturing
1	R38	30.1 kΩ resistor precision thick film chip, R0603	ERJ-3EKF3012V	Panasonic
1	R39	75 kΩ resistor precision thick film chip, 0603	ERJ-3EKF7502V	Panasonic
1	R44	649 kΩ resistor precision thick film chip, automotive grade	ERJ-2RKF6493X	Panasonic
1	R45	210 kΩ resistor precision thin film chip	CPF0402B210KE1	Te Connectivity
1	R46	953 kΩ resistor chip SMD, 0805	9C08052A9533FKHFT	Yageo
1	R47	200 kΩ resistor precision thick film chip	ERJ-2RKF2003X	Panasonic
3	R53, R58, R60	33 Ω resistors, film SMD, 0603	MC 0.063W 0603 1% 33R	Multicomp
1	R54	49.9 Ω resistor precision thick film chip, R0603	ERJ-3EKF49R9V	Panasonic
2	R56, R57	1 kΩ resistors, precision thick film chip, R0603	ERJ-3EKF1001V	Panasonic
1	R74	4.12 kΩ resistor precision thick film chip	ERJ-2RKF4121X	Panasonic
1	R76	Do not install	TBD0402	TBD0402
1	R79	10 Ω resistor precision thick film chip, R0603	ERJ-3EKF10R0V	Panasonic
1	R80	91 Ω resistor thick film chip	RC0603FR-0791RL	Yageo
1	R84	2.4 kΩ resistor precision thick film chip, 0603	ERJ-3EKF2401V	Panasonic
1	T1	Transformer RF1:1	MABA-007159-000000	Macom Technology Solutions
1	U1	16-/18-bit, 15 MSPS, µModule data acquisition solutions	ADAQ23876BBCZ/ ADAQ23878BBCZ	Analog Devices
1	U10	D-type positive edge	NL17SZ74USG	ON Semiconductor
1	U11	Low voltage dual supply, 2-bit signal translator	FXL2TD245L10X	ON Semiconductor
2	U9, U12	CMOS tiny logic high speed inverters	NC7S04M5X	Fairchild Semiconductor
1	U13	800 MHz clock distribution	AD9513BCPZ	Analog Devices
1	U14	2 kB serial i^2c bus EEPROM, 1.8 V to 5.5 V	M24C02-RMN6TP	ST Microelectronics
1	U3	Ultralow noise, high accuracy voltage reference	ADR4520ARZ	Analog Devices
1	U4	Low noise, CMOS LDO linear regulator	ADP7118AUJZ-2.5-R7	Analog Devices
1	U5	0.25 ppm noise, low drift precision references, 4.096 voltage output	LTC6655BHMS8-4.096#PBF	Analog Devices
1	U6	Dual SEPIC or inverting µModule dc-to-dc converter	LTM8049EY#PBF	Analog Devices
1	U7	Ultralow noise, high power supply rejection ratio (PSRR), LDO, adjustable voltage output	ADP7183ACPZN-R7	Analog Devices
1	U8	Low dropout, low noise, micropower regulator	LT3023IDD#PBF	Analog Devices
2	VIN+, VIN-	Connector PCB end launch SMA edge mount	142-0761-841	Cinch Connectivity
1	Y1	Crystal ultralow phase noise oscillator	CCHD-575-50-100.000	Crystek Corporations
11	Headers	Shunt, 1.27 mm pitch black with handle	M50-2000005	Harwin
10	+2P5V, +5V, +6P5V, +7V, -2P5V, -2V,3P3VAX, TP15, TSTMOD, TSTPAT	Connector PCB test points, red	5000	Keystone Electronics
7	C12, C23, C24, C25, C29, C39, C40	Do not install	TBD0402	TBD0402
2	C15, C16	0.1 µF ceramic capacitors, X7R	06035C104J4Z2A	AVX
4	C5, C6, C79, C80	Do not install	TBD0603	TBD0603
3	J1, J2, J4	Connector PCB straight SMA die cast	5-1814832-2	Te Connectivity, Ltd.
14	R1, R2, R4, R5, R12, R23, R31, R32, R49, R88, R89, R90, R91, R92	0 Ω resistors, film SMD, R0603	MC0603WG00000T5E-TC	Multicomp
4	R17 to R20	0 Ω resistors, high power and precision metal film chip	RGH1608-2C-P-820-B	Susumu Co., Ltd.
1	R3	Do not install	TBD0603	TBD0603
4	R43, R50, R51, R75	Do not install	TBD0402	TBD0402

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.