



PMX100UN

20 V, N-channel Trench MOSFET

2 December 2021

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN0603-3 (SOT8013) Surface-Mounted Device (SMD) using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Leadless ultra small package; 0.63 x 0.33 x 0.25 mm
- Trench MOSFET technology
- Low profile (0.25 mm)

3. Applications

- Battery switch
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

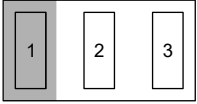
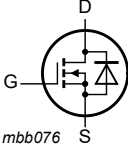
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	20	V
V_{GS}	gate-source voltage			-12	-	12	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-	1.3	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 1\text{ A}; T_j = 25\text{ °C}$		-	122	210	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN0603-3 (SOT8013)	
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMX100UN	DFN0603-3	DFN0603-3; plastic, ultra small and leadless full encapsulated package; 3 terminals; 0.225 mm pitch; 0.63 mm x 0.33 mm x 0.25 mm body	SOT8013

7. Marking

Table 4. Marking codes

Type number	Marking code
PMX100UN	R

8. Limiting values

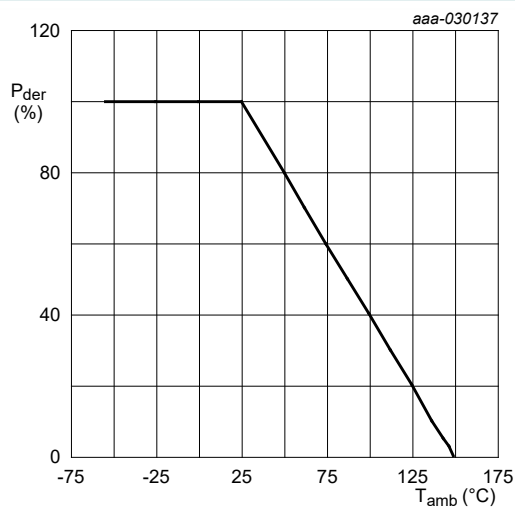
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	20	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	1.3	A
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	0.8	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	5.2	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	300	mW
			[1]	-	500	mW
		T _{sp} = 25 °C		-	4.7	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	0.5	A

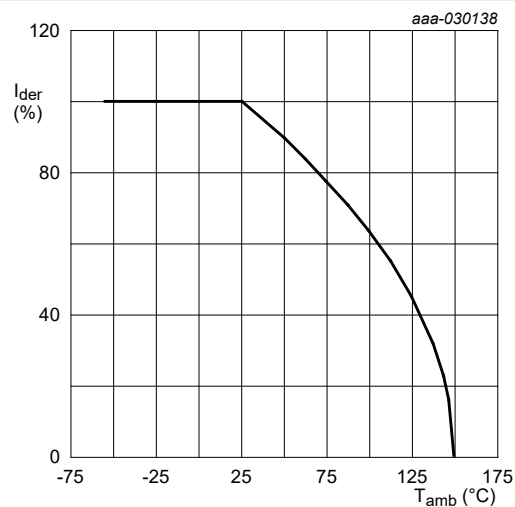
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}\text{C})} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_D(25^{\circ}\text{C})} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of ambient temperature

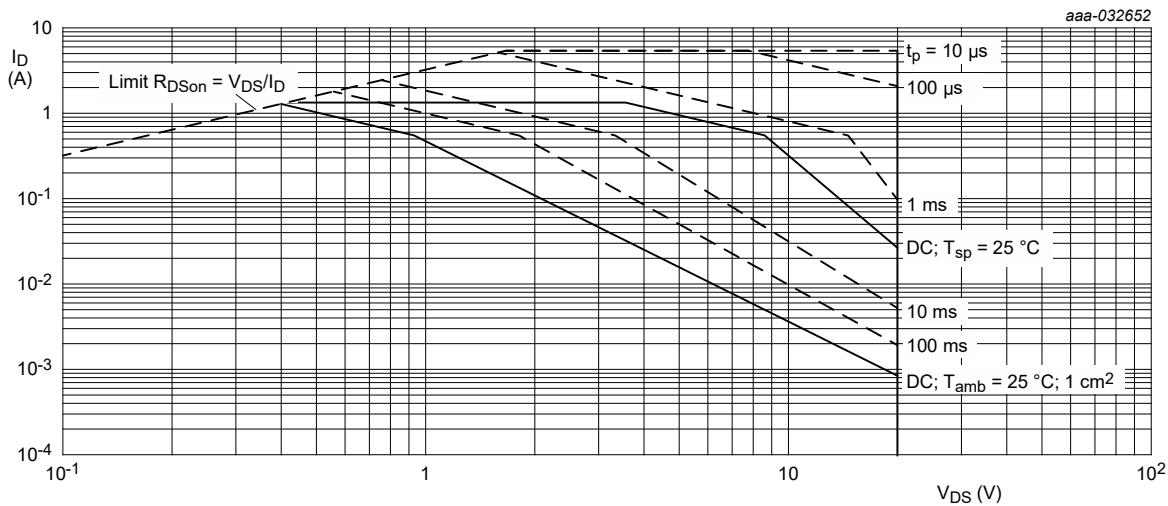


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	360	415	K/W
			[2]	-	215	250	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	23	26.5	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

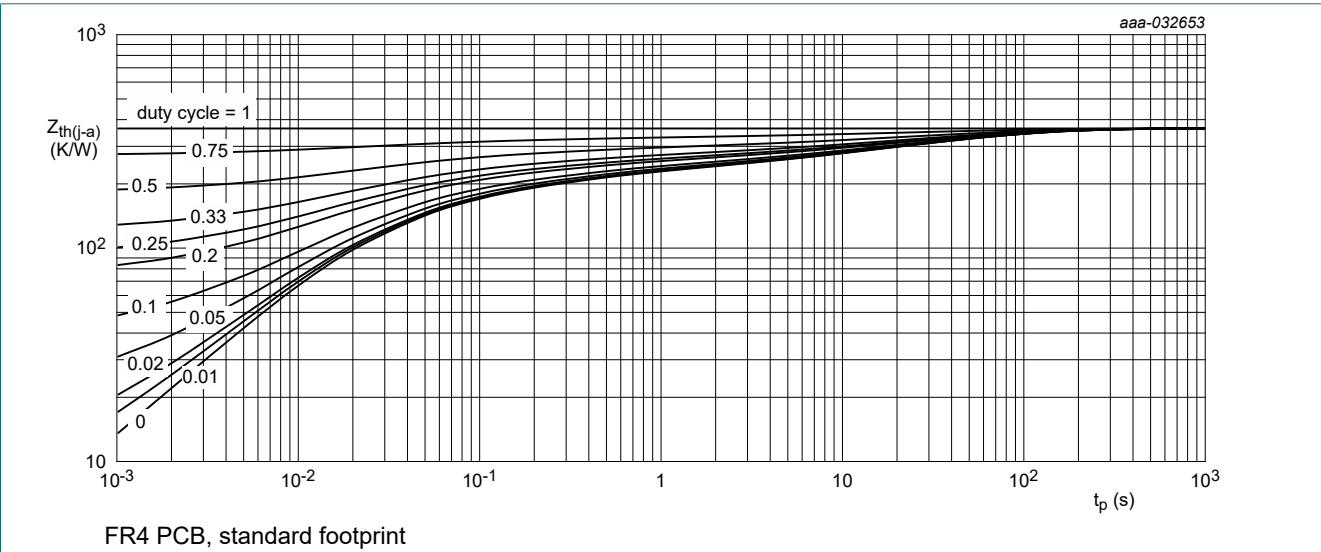


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

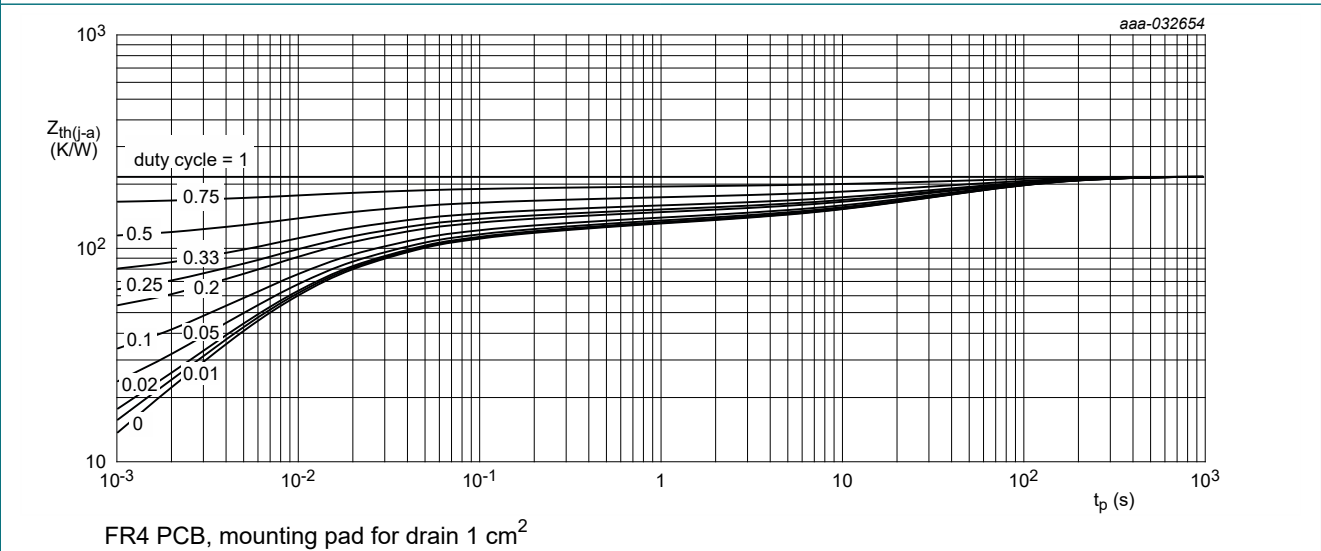


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		0.5	0.7	0.9	V
I _{DSS}	drain leakage current	V _{DS} = 20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 1 A; T _j = 25 °C		-	122	210	mΩ
		V _{GS} = 4.5 V; I _D = 1 A; T _j = 150 °C		-	184	320	mΩ
		V _{GS} = 2.5 V; I _D = 1 A; T _j = 25 °C		-	160	230	mΩ
		V _{GS} = 1.8 V; I _D = 0.5 A; T _j = 25 °C		-	233	360	mΩ
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 1 A; T _j = 25 °C		-	2.5	-	S
R _G	gate resistance	f = 1 MHz		-	11	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = 10 V; I _D = 1.3 A; V _{GS} = 4.5 V; T _j = 25 °C		-	1.5	2.3	nC
Q _{GS}	gate-source charge			-	0.2	-	nC
Q _{GD}	gate-drain charge			-	0.4	-	nC
C _{iss}	input capacitance	V _{DS} = 10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	144	-	pF
C _{oss}	output capacitance			-	14	-	pF
C _{rss}	reverse transfer capacitance			-	12	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 10 V; I _D = 1 A; V _{GS} = 4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	1	-	ns
t _r	rise time			-	2	-	ns
t _{d(off)}	turn-off delay time			-	4	-	ns
t _f	fall time			-	1	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 0.5 A; V _{GS} = 0 V; T _j = 25 °C		-	0.8	1.2	V

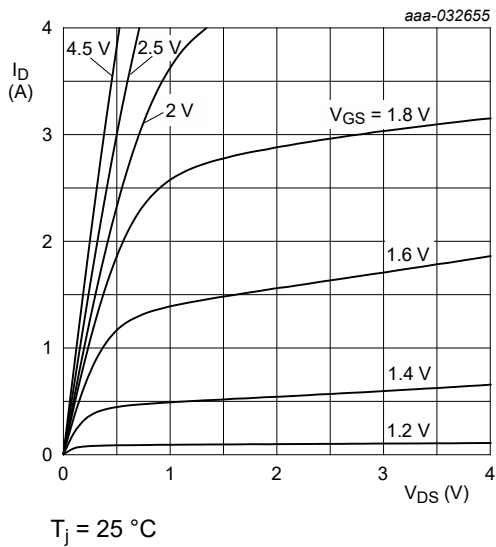


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

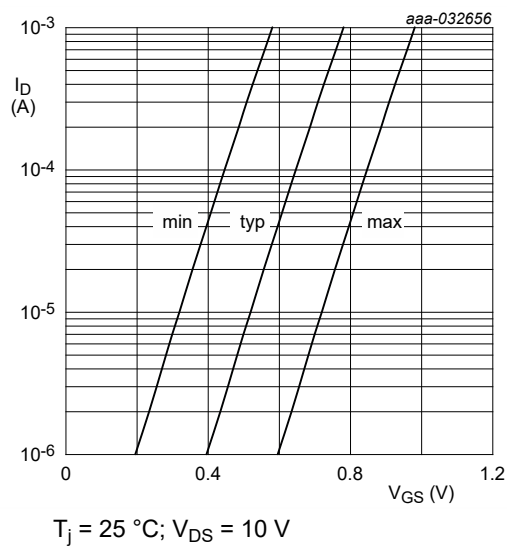


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

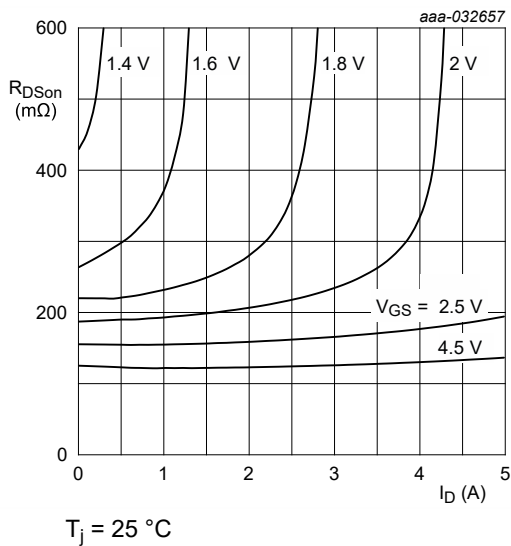


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

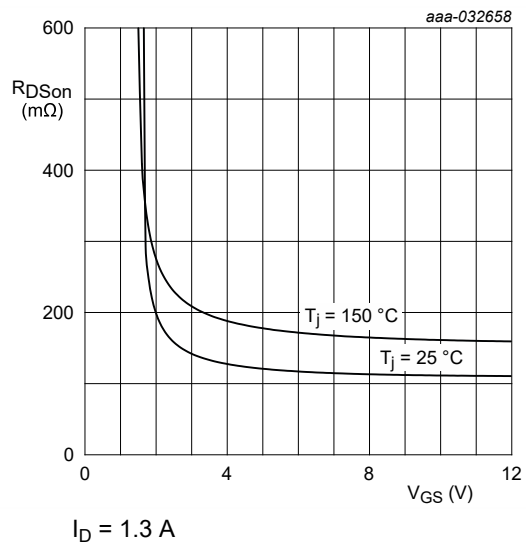


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

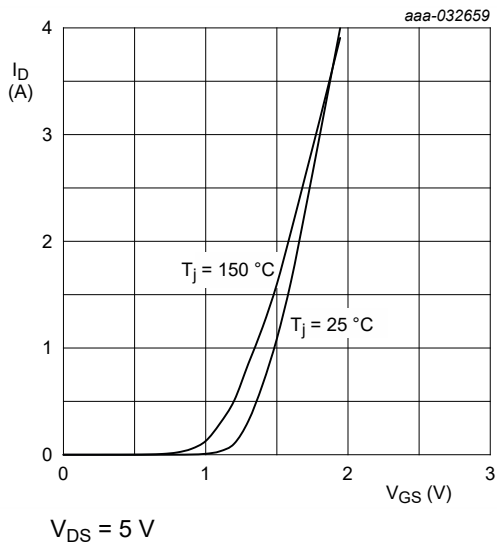


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

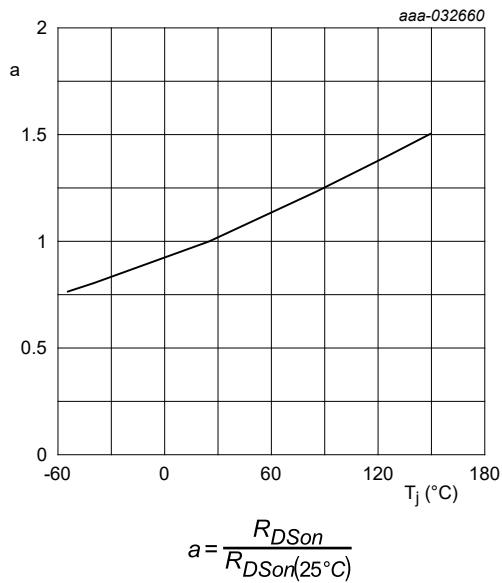


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

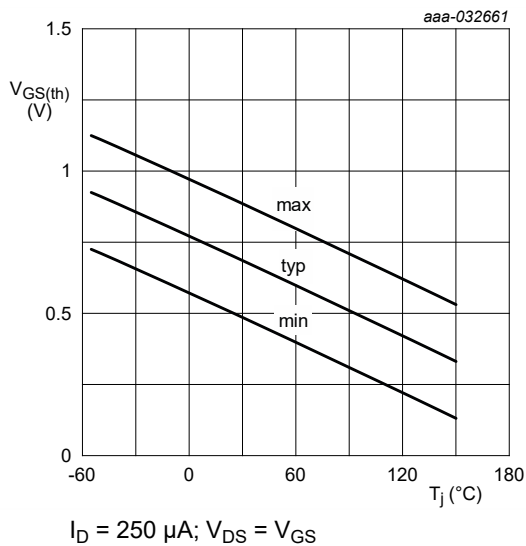


Fig. 12. Gate-source threshold voltage as a function of junction temperature

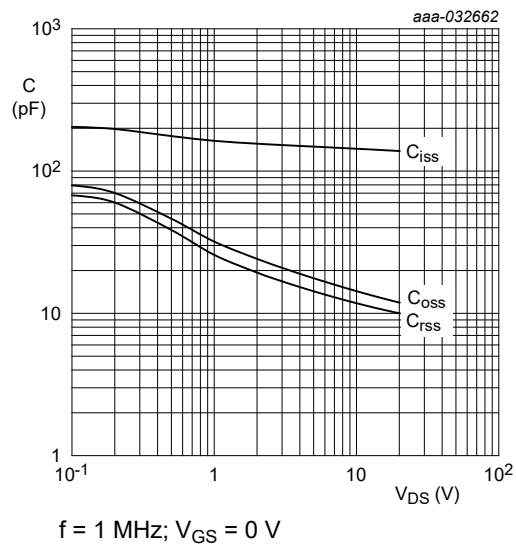


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

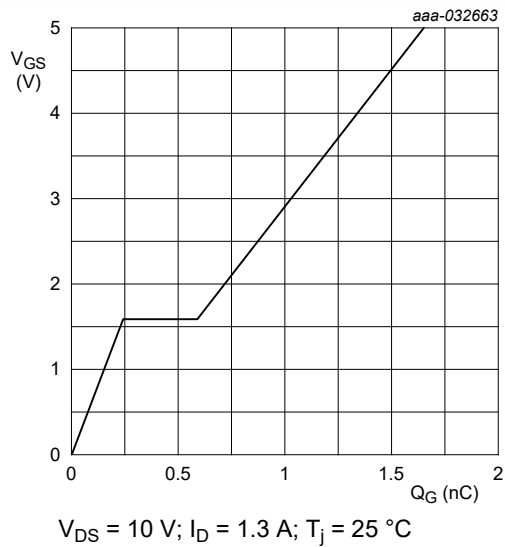


Fig. 14. Gate-source voltage as a function of gate charge; typical values

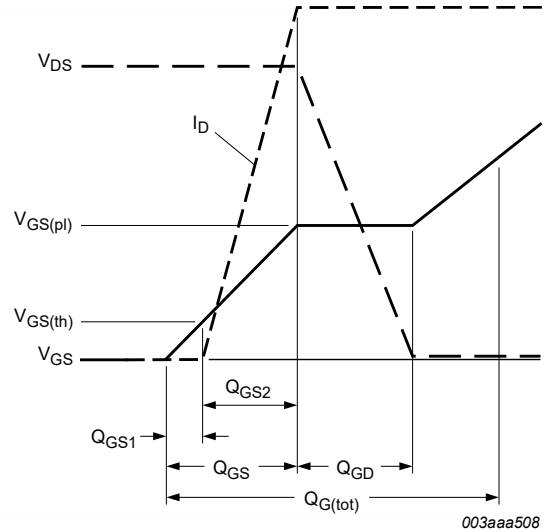


Fig. 15. Gate charge waveform definitions

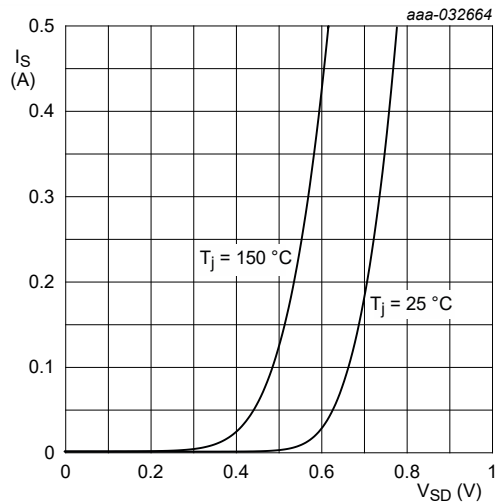


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

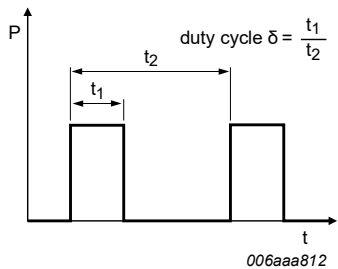


Fig. 17. Duty cycle definition

12. Package outline

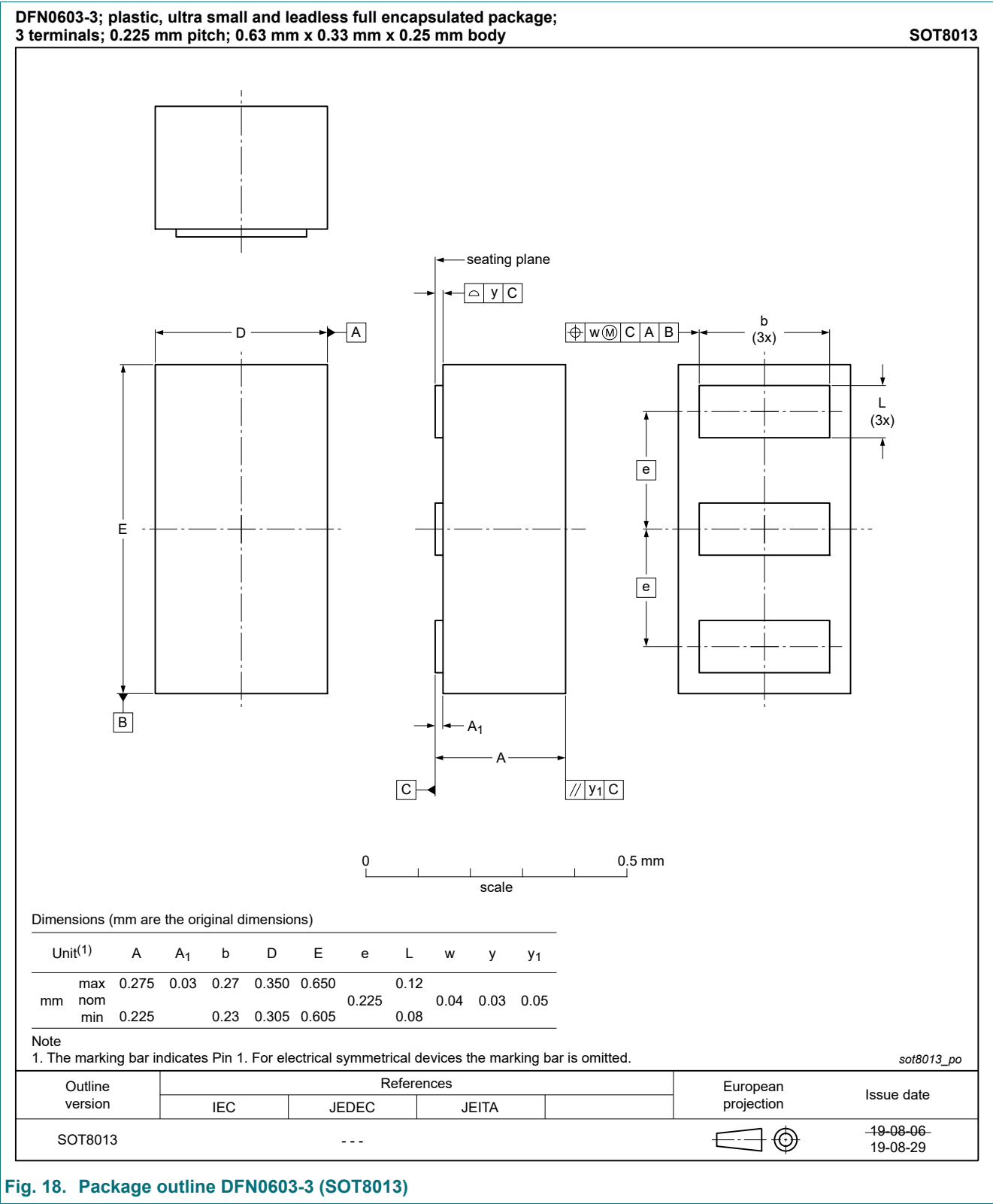


Fig. 18. Package outline DFN0603-3 (SOT8013)

13. Soldering

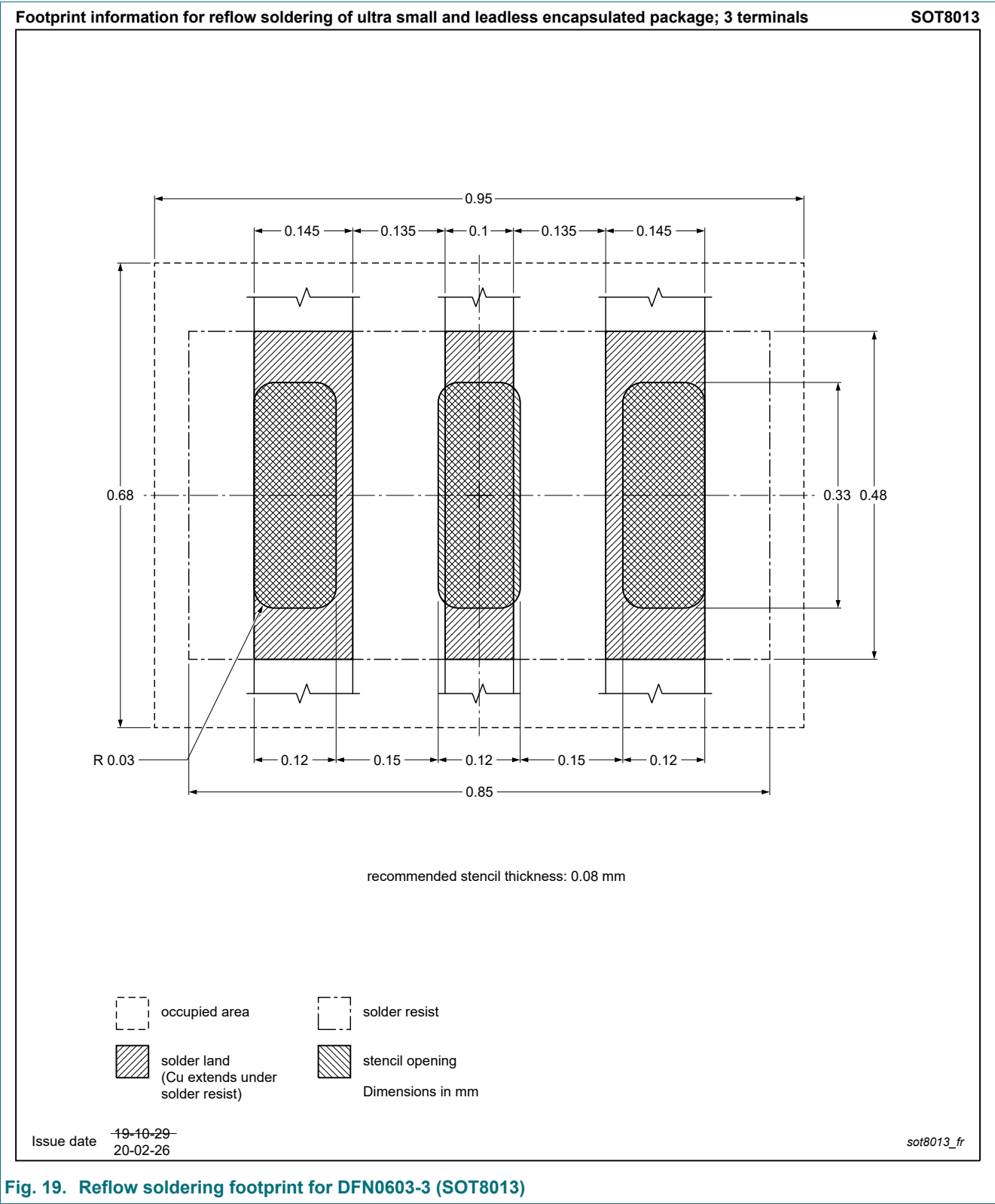


Fig. 19. Reflow soldering footprint for DFN0603-3 (SOT8013)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMX100UN v.2	20211202	Product data sheet	-	PMX100UN v.1
Modifications:	Chapter "Characteristics": typo correction on Fig. 16			
PMX100UN v.1	20210407	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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