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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E43RA-FW430-C

Overview:

- 4.3-inch TFT: (115.4x79.15 mm)
- 480(RGB)x272 pixels
- 16/18/24-bit RGB Interface
- Top View/Wide Temp
- White LED back-light
- Transmissive/ Normally White
- Capacitive Touch Panel
- 430 NITS
- Controller: ST7282
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit, capacitive touch panel and backlight unit. The resolution of the 4.3" TFT-LCD contains 480x272 pixels and can display up to 65K/262K/16.7M colors.

TFT Features

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	95.04 (H) x 53.86 (V) (4.3 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	480(RGB)x272	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.198 (H) x 0.198 (V)	mm	-
Viewing angle	12:00	o'clock	-
TFT Controller IC	ST7282	-	-
LCM Interface	16/18/24-bit RGB	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-
Module Bonding	Tape bonding between LCM CTP	-	-

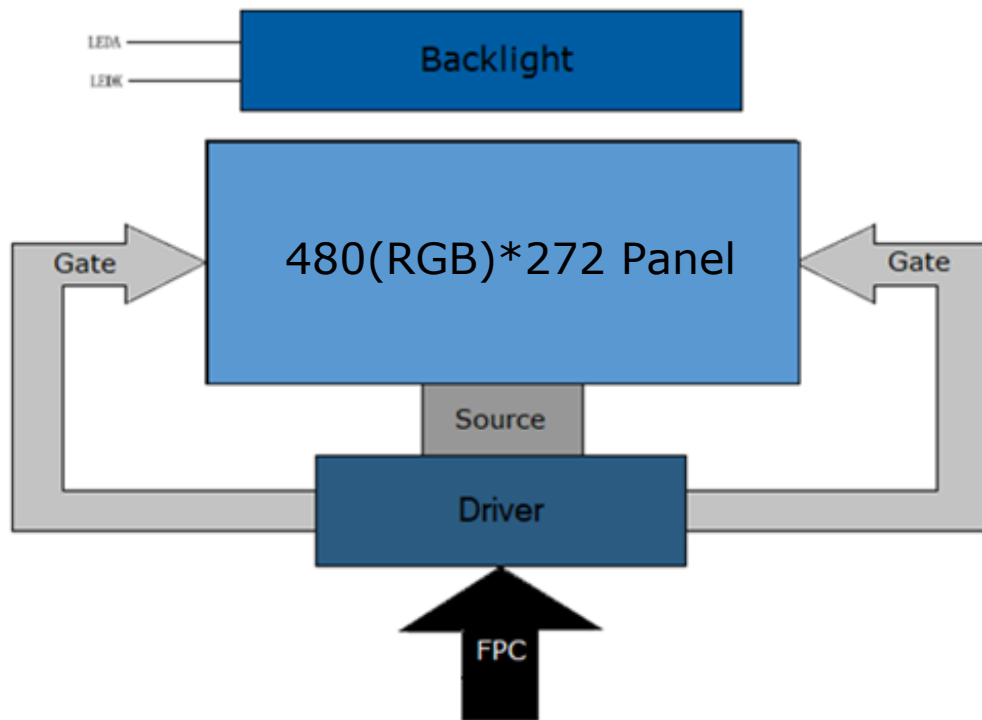
CTP Features

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	480(H)*272(V)	-	-
Structure	G+G	-	-
Controller IC	GT911	-	-
Interface	I2C	-	-
Slave Address	0x5D(7bit) or 0x14(7bit)	-	-
Touch Mode	Five Points and Gestures	-	-

Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	Height (H)		115.4		mm	-
	Vertical (V)		79.15		mm	-
	Depth (D)		4.79		mm	-
Weight			TBD		g	-

1. Block Diagram



3. Input Terminal Pin Assignment

Recommended TFT Connector: FH12S-40S-0.5SH(55)

Recommended CTP Connector: FH12-8S-0.5SH(55)

NO.	Symbol	Description	I/O
1	LEDK	Cathode pin of backlight	P
2	LEDA	Anode pin of backlight	P
3	GND	Ground	P
4	VDD	Supply voltage (3.3V)	P
5-12	R0-R7	8-bit digital red data input	I
13-20	G0-G7	8-bit digital green data input	I
21-28	B0-B7	8-bit digital blue input	I
29	GND	Ground	P
30	PCLK	Clock signal. Latching data at falling edge.	I
31	DISP	Display control/ standby mode selection DISP = "low", standby mode (default) DISP = "high", normal display mode	I
32	HSYNC	Horizontal sync signal. Negative polarity.	I
33	VSYNC	Vertical sync signal. Negative polarity.	I
34	DE	Data input enable. Active high to enable the data input. When not used in SYNC mode, connect to low.	I
35	NC	Not connected	--
36	GND	Ground	P
37	XR(NC)	Touch panel right glass terminal	A/D
38	YD(NC)	Touch panel bottom film terminal	A/D
39	XL(NC)	Touch panel left glass terminal	A/D
40	YU(NC)	Touch panel top film terminal	A/D

I: Input, O: Output, P: Power

3.1 CTP

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	NC	Not connected	--
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to host	I
7	RST	External reset. Low is active.	I
8	GND	Ground	P

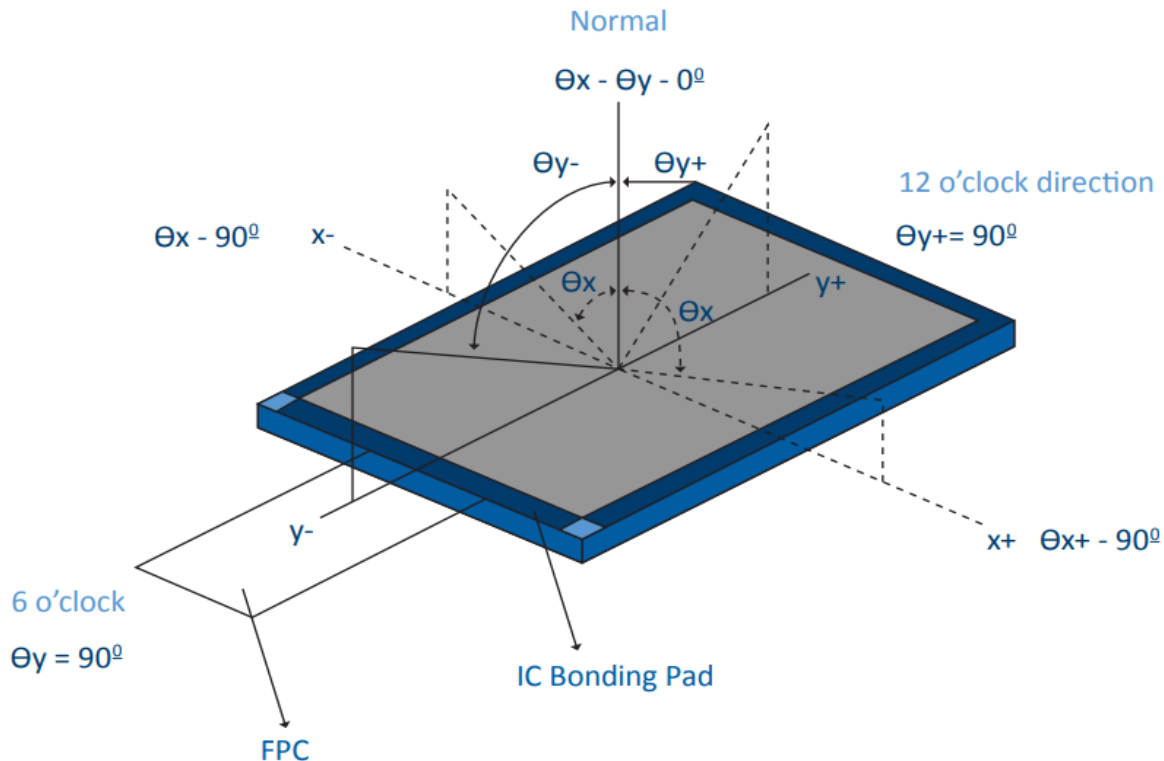
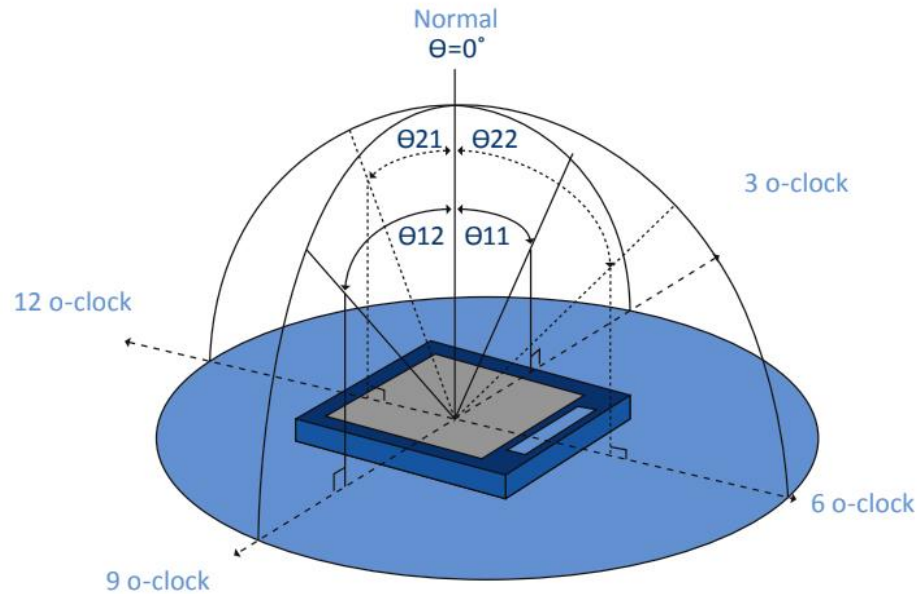
4. LCD Optical Characteristics

4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	$\theta=0$ Normal viewing angle	--	350	--	%	(2)
Response Time	Rising	TR+TF		--	30	45	msec	(4)
	Falling							
Color Gamut		S(%)		--	50	--	%	(5)
Color Filter Chromaticity	White	W_x		0.241	0.281	0.321		(5)(6)
		W_y		0.248	0.288	0.328		
	Red	R_x		0.543	0.583	0.623		
		R_y		0.291	0.331	0.371		
	Green	G_x		0.299	0.339	0.379		
		G_y		0.570	0.610	0.650		
	Blue	B_x		0.115	0.155	0.195		
		B_y		0.035	0.075	0.115		
Viewing angle	Hor.	θ_L	CR $\geq$ 10	--	70	--	degree	(1)(6)
		θ_R		--	70	--		
	Ver.	θ_T		--	60	--		
		θ_B		--	70	--		
Option View Direction		12:00 o'clock						(1)

Optical Specification Reference Notes:

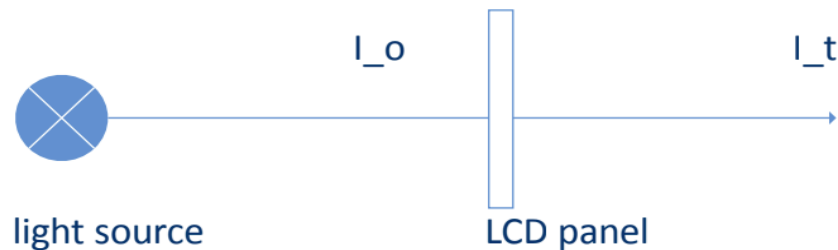
(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.



(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (L_w) in a full white area ($R=G=B=1$) and the luminance (L_d) in a dark area ($R=G=B=0$).

$$Cr = \frac{L_w}{L_d}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.



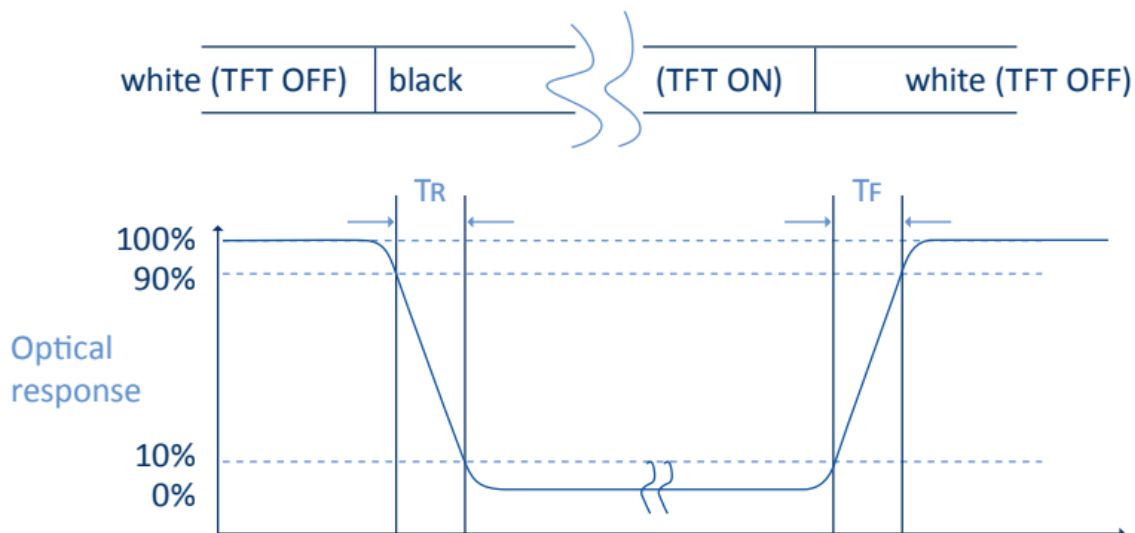
The transmittance is defined as:

$$Tr = \frac{I_t}{I_o} \times 100\%$$

I_o = the brightness of the light source.

I_t = the brightness after panel transmission

(4) Definition of Response Time (T_r , T_f): The rise time ' T_r ' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time ' T_f ' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y), G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

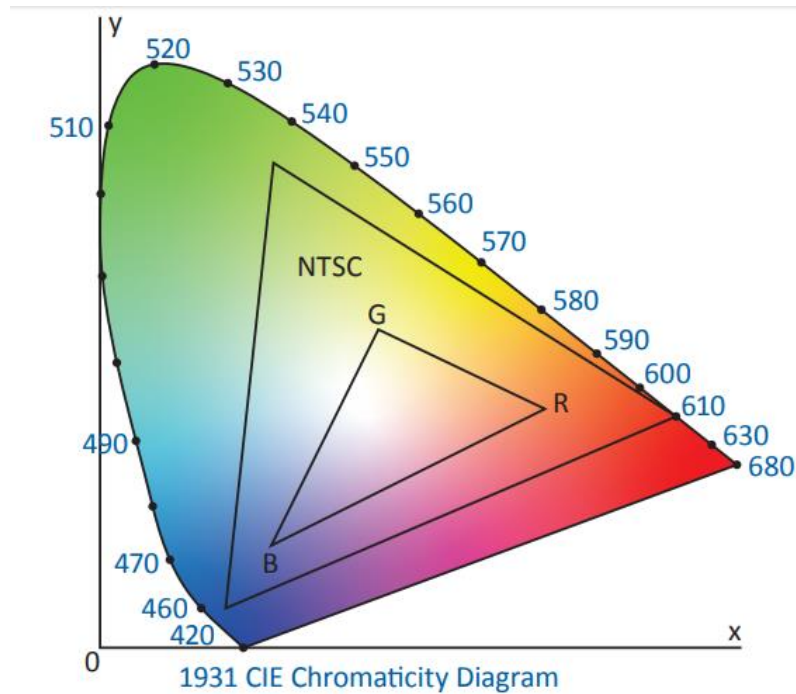
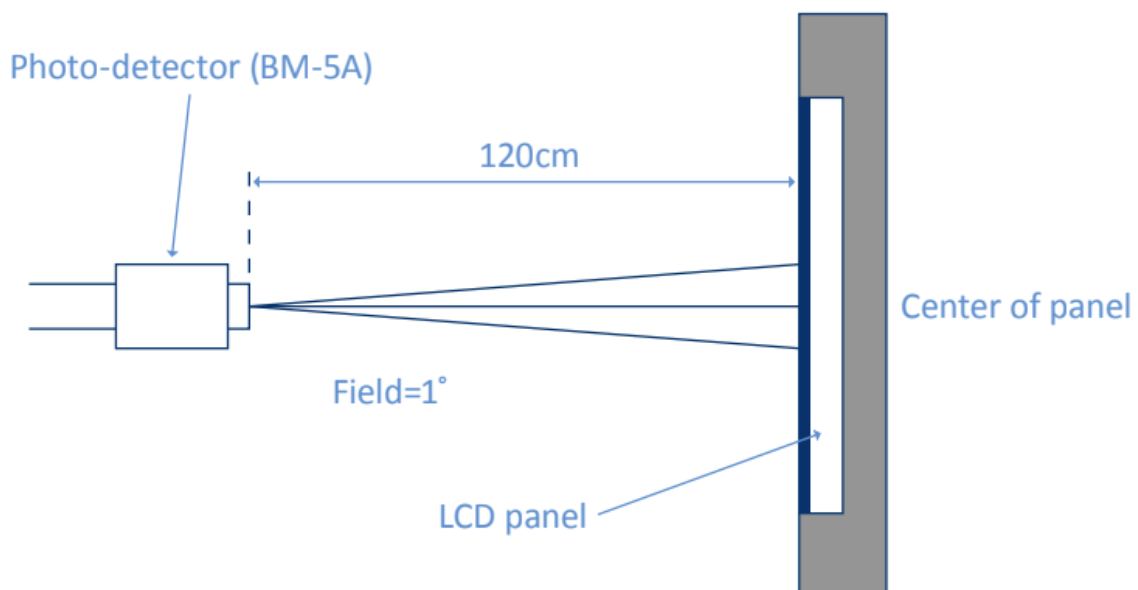


Fig. 1931 CIE chromacity diagram

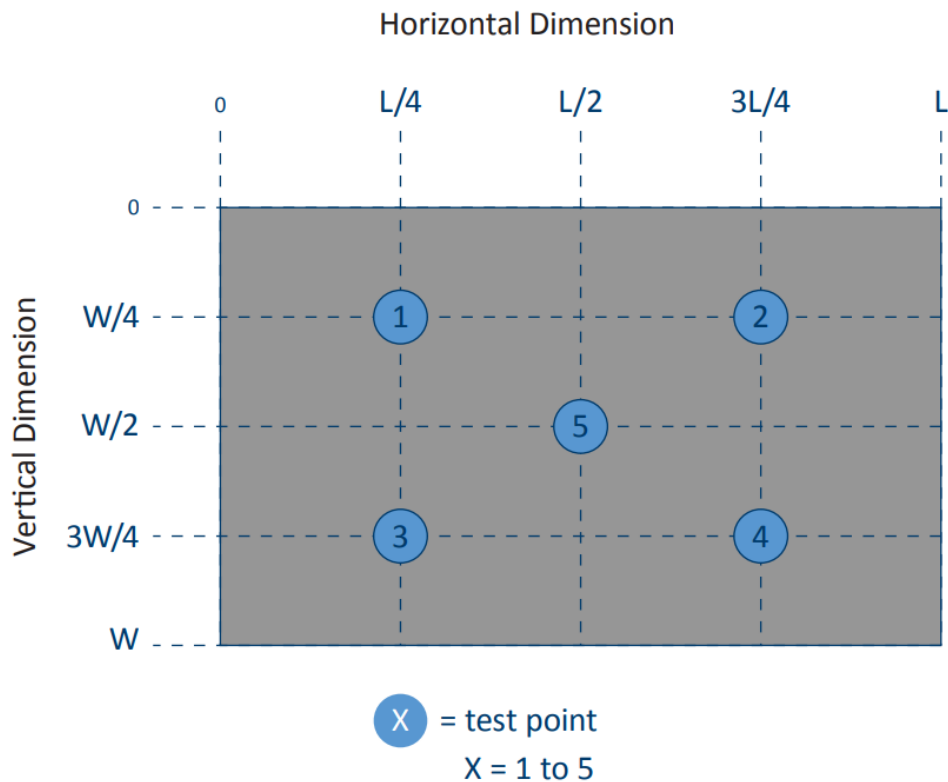
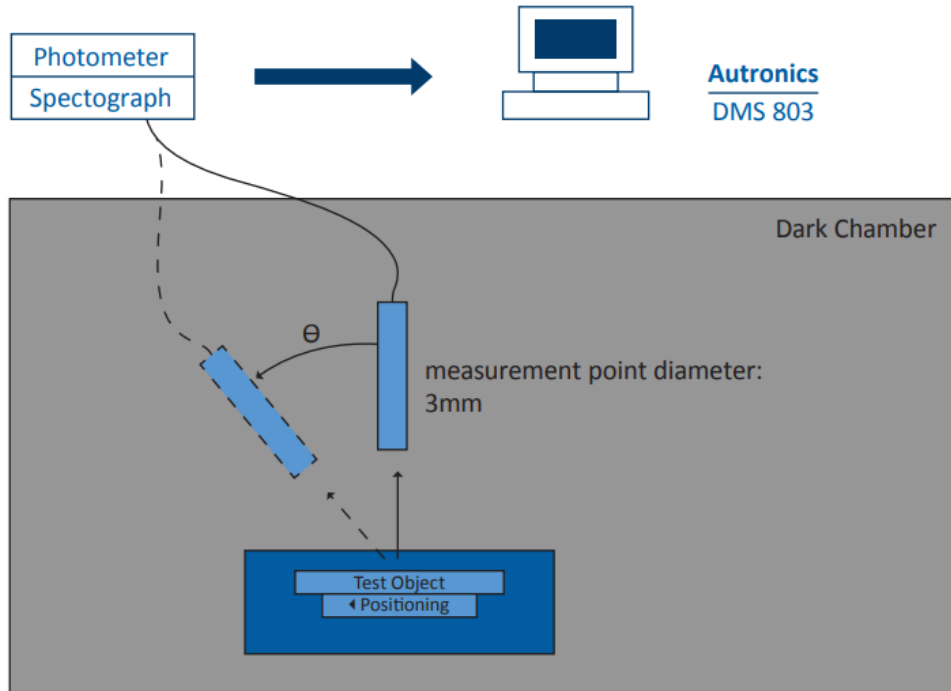
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.



5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 °C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Operating Temperature	TOP	-20	+70	°C
Storage Temperature	TST	-30	+80	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VDD	3.0	3.3	3.6	V	
Normal Mode Current Consumption	IDD	--	25	--	mA	
Level Input Voltage	VIH	0.7VDD	--	VDD	V	
	VIL	GND	--	0.3VDD	V	
Level Output Voltage	VOH	VDD-0.4	--	VDD	V	
	VOL	GND	--	GND+0.4	V	

5.3 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	15	20	--	mA	
Forward Voltage	VF	--	28.8	--	V	
LCM Luminance	LV	380	430	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 9 chips White LED.

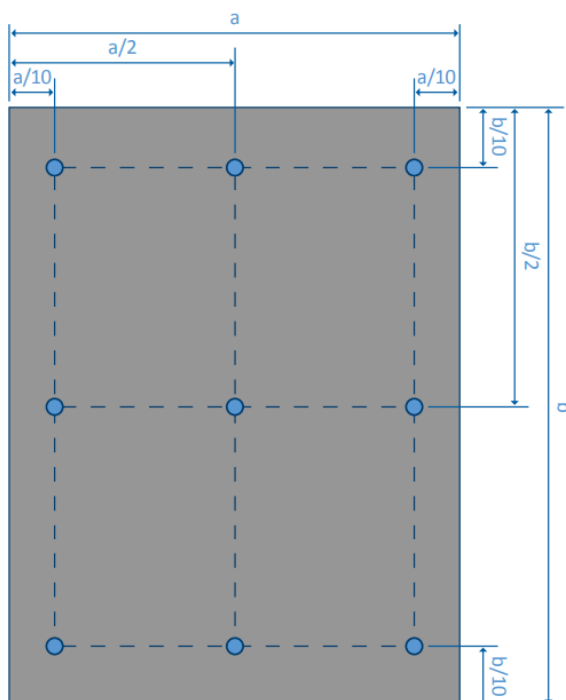
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED lifetime” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{(\text{Total Luminance of 9 points})}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. AC Characteristics

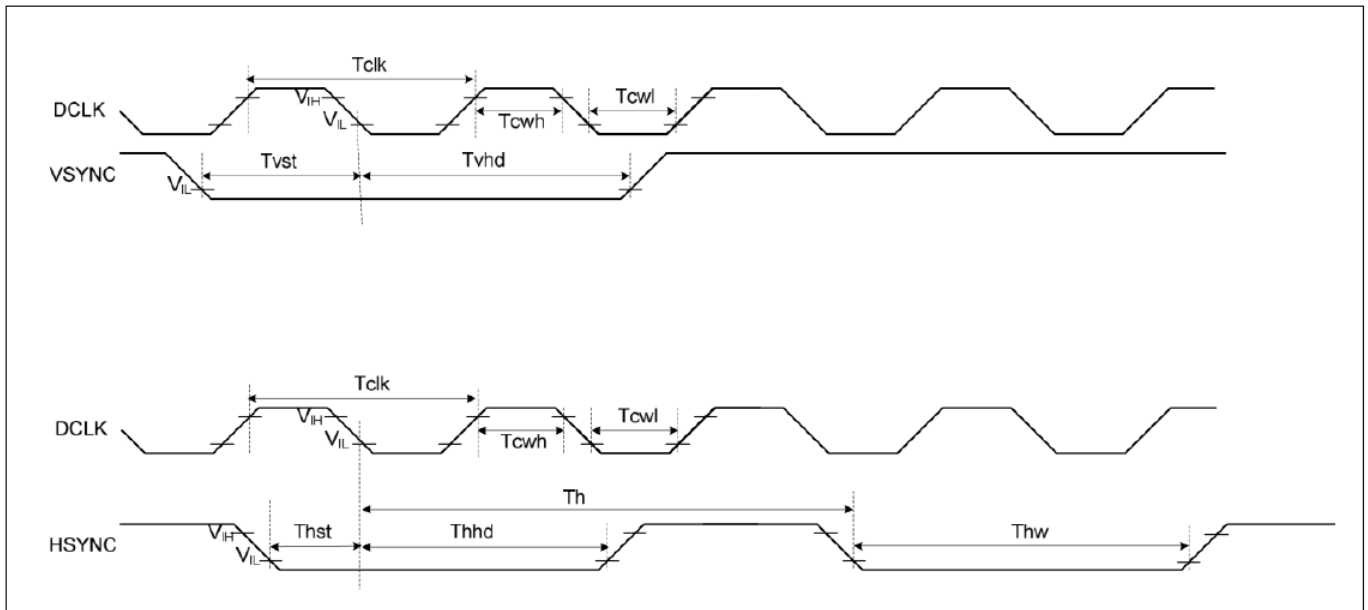
6.1 Input Signal Characteristics

AC Electrical Characteristics (VDDIO=VDD=3.0 to 3.6V, GND=0V, TA=-20 to +85 °C)

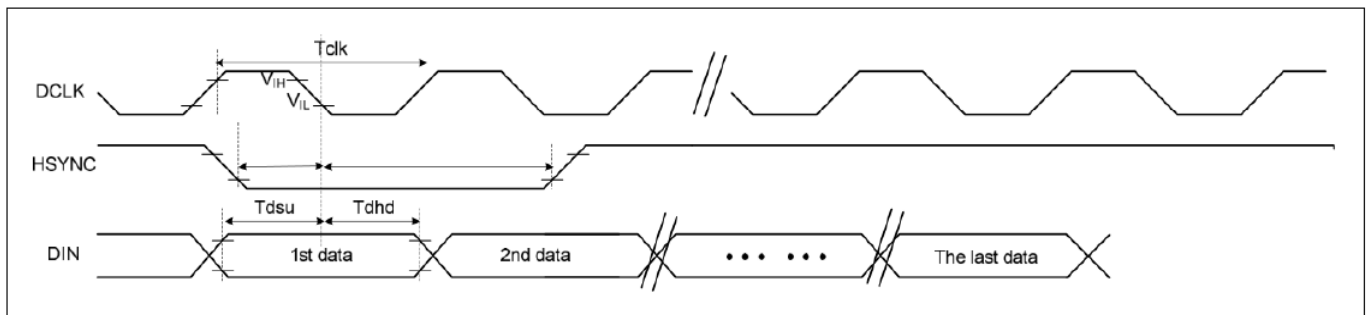
Item	Symbol	Min	Typ.	Max	Unit	Conditions
System operation timing						
VDD power source slew time	TPO	-	-	20	ms	From 0V to 99% VDD
GRB pulse width	tRSTW	10	50	-	us	R=10kΩ, C=1uF
Input/output timing						
CLK pulse duty	Tcw	40	50	60	%	
Hsync width	Thw	1	-	-	DCLK	
Hsync period	Th	55	60	65	us	
Vsync setup time	Tvst	12	-	-	ns	
Vsync hold time	Tvhd	12	-	-	ns	
Hsync setup time	Thst	12	-	-	ns	
Hsync hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
SD output stable time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF
GD output rise and fall time	Tgst	-	-	6	us	Output settled (5%-95%) Loading = 4.7k+29.8pF
3-wire serial communication						
Delay between CSB and Vsync	Tcv	1	-	-	us	
CS input setup time	Ts0	50	-	-	ns	
Serial data input setup time	Ts1	50	-	-	ns	
CS input hold time	Th0	50	-	-	ns	
Serial data input hold time	Th1	50	-	-	ns	
SCL pulse high width	Twh1	50	-	-	ns	
SCL pulse low width	Twl1	50	-	-	ns	
CS pulse high width	Tw2	400	-	-	ns	

6.2 AC Timing Diagrams

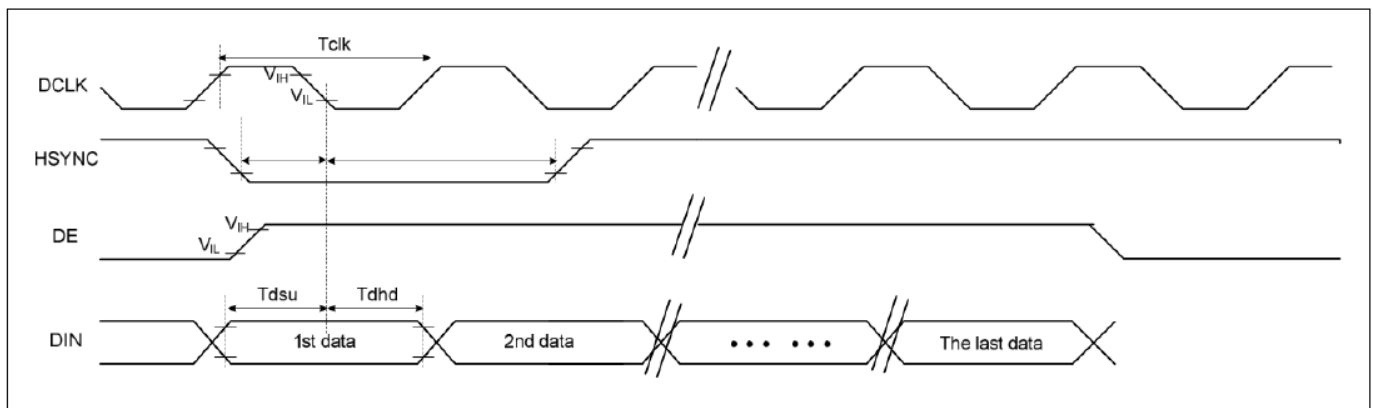
6.2.1 Clock and Data Input Timing



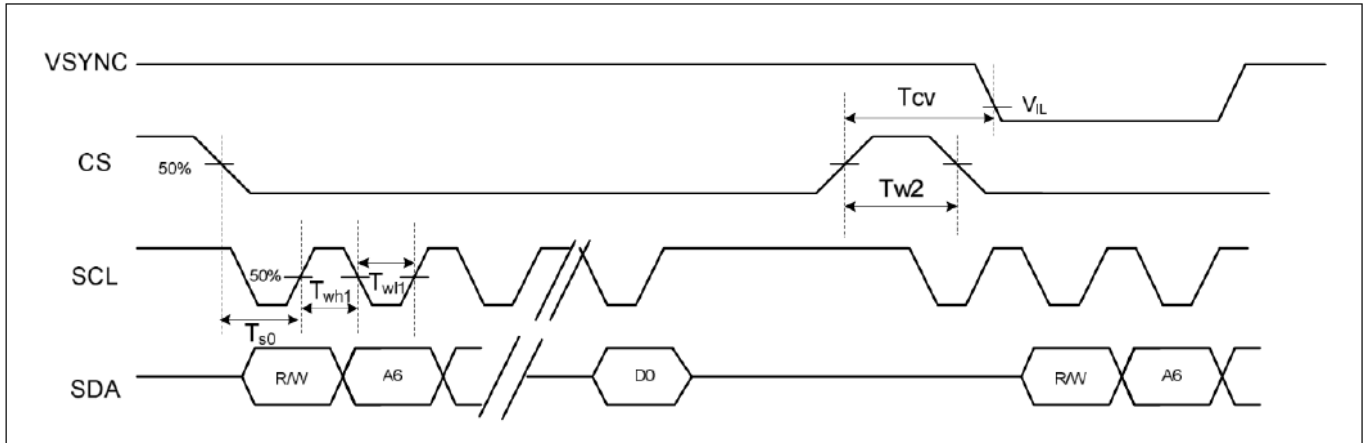
6.2.2 SYNC Mode



6.2.3 SYNC DE-Mode



6.3 3-Wire Communication Timing Diagram



6.4 RGB Input Timing Table

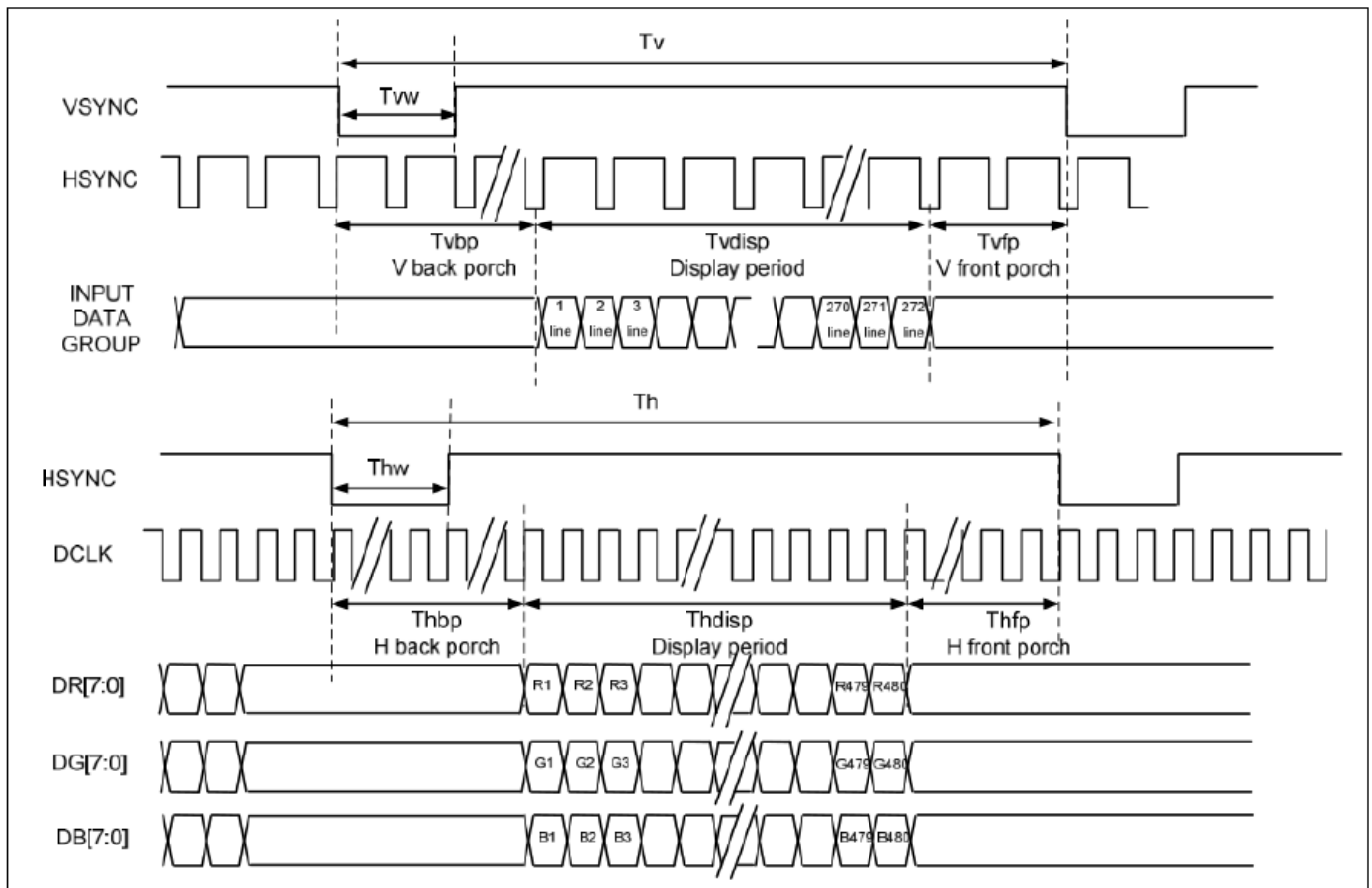
6.4.1 Parallel 24-bit RGB Timing Table

Item		Symbol	Min	Typ.	Max	Unit	Conditions
DCLK Frequency		Fclk	8	9	12	MHz	
DCLK Period		Tclk	83	111	125	ns	
HSYNC	Period Time	Th	485	525	532	DCLK	
	Display Period	Thdisp	-	480	1	DCLK	
	Back Porch	Thbp	3	43	50	DCLK	By H_Blanking setting
	Front Porch	Thfp	2	2	2	DCLK	
	Pulse Width	Thw	1	1	1	DCLK	
VSYNC	Period Time	Tv	275	285	303	H	
	Display Period	Tvdisp	-	272	-	H	
	Back Porch	Tvbp	2	12	30	H	By V_Blanking setting
	Front Porch	Tvfp	1	1	1	H	
	Pulse Width	Tvw	1	1	1	H	

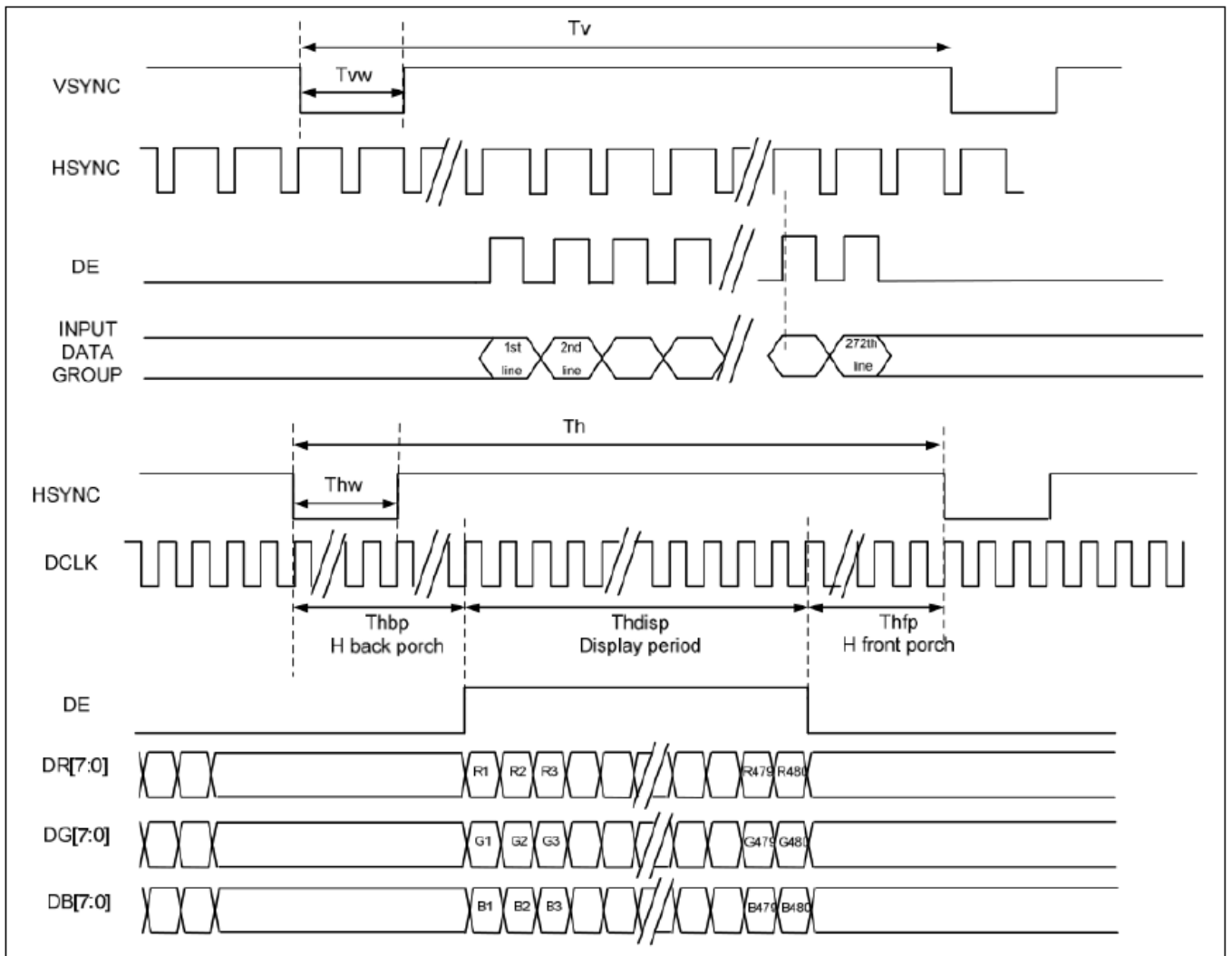
6.4.2 Series 8-bit RGB Timing Table

Item		Symbol	Min	Typ.	Max	Unit	Conditions
DCLK Frequency		Fclk	24	27	30	MHz	
DCLK Period		Tclk	33	37	42	ns	
HSYNC	Period Time	Th	1560	1716	1900	DCLK	
	Display Period	Thdisp	-	1440	-	DCLK	
	Back Porch	Thbp	108	129	255	DCLK	By H_Blanking setting
	Front Porch	Thfp	12	147	205	DCLK	
	Pulse Width	Thw	1	1	50	DCLK	
VSYNC	Period Time	Tv	274	288	335	H	
	Display Period	Tvdisp	-	272	-	H	
	Back Porch	Tvbp	1	12	32	H	By V_Blanking setting
	Front Porch	Tvfp	1	4	31	H	
	Pulse Width	Tvw	1	10	30	H	

6.5 SYNC Mode Timing Diagram



6.6 SYNC-DE Mode Timing Diagram



7. CTP Electrical Characteristics

7.1 Absolute Maximum Rating

Characteristics	Symbol	Min	Max	Unit
Power Supply Voltage	VDD	2.66	3.47	V
I/O Digital Voltage	VDDIO	--	--	V
Operating Temperature	TOP	-20	+70	°C
Storage Temperature	TST	-30	+80	°C

Table 7.1: CTP Absolute Maximum Rating Characteristics

NOTE: If used beyond the absolute maximum ratings, GT911 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the conditions not within the electrical characteristics, it may affect the reliability of the device.

7.2 DC Electrical Characteristics (Ta=25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	VDD	2.66	3.3	3.47	V
Doze Mode Operating Current	I _o	--	0.78	--	mA
Normal Operation Mode Current Consumption	I _{opr}	--	8	14.5	mA
Green Mode Current Consumption	I _{mon}	--	3.3	--	mA
Sleep Mode Current Consumption	I _{slp}	70	--	120	uA
Level Input Voltage	V _{IH}	0.75VDD	--	VDD+0.3	V
	V _{IL}	-0.3	--	0.25VDD	V
Level Output Voltage	V _{OH}	0.85VDD	--	--	V
	V _{OL}	--	--	0.15VDD	V

Table 7.2: CTP DC Electrical Characteristics

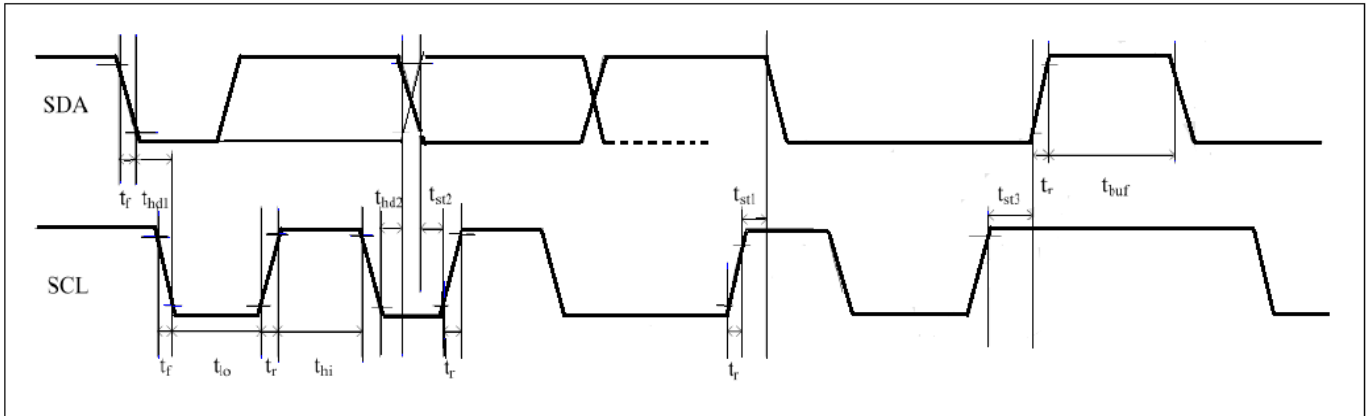
7.3 AC Characteristics

Parameter	Min	Typ.	Max	Unit
OSC oscillation frequency	59	60	61	MHz
I/O output rise time, low to high	--	14	--	ns
I/O output fall time, high to low	--	14	--	ns

Table 7.3: CTP AC Electrical Characteristics

7.4 I2C Interface Characteristics

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is recommended that transmission rate be kept at or below 400kbps. The figure shown below is the I2C timing:



Parameter	Symbols	Condition	Min	Max	Units
SCL low period	t_{lo}		1.3		us
SCL high period	t_{hi}		0.6		us
SCL setup time for start condition	t_{st1}		0.6		us
SCL setup time for stop condition	t_{st3}		0.6		us
SCL hold time for start condition	t_{hd1}		0.6		us
SDA setup time	t_{st2}		0.1		us
SDA hold time	t_{hd2}		0		us

Table 7.4: I2C AC Characteristics, 1.8V interface voltage, 400kbps transmission rate, 2k pull-up resistor

Parameter	Symbols	Condition	Min	Max	Units
SCL low period	t_{lo}		1.3		us
SCL high period	t_{hi}		0.6		us
SCL setup time for start condition	t_{st1}		0.6		us
SCL setup time for stop condition	t_{st3}		0.6		us
SCL hold time for start condition	t_{hd1}		0.6		us
SDA setup time	t_{st2}		0.1		us
SDA hold time	t_{hd2}		0		us

Table 7.5: I2C AC Characteristics, 3.3V interface voltage, 400kbps transmission rate, 2k pull-up resistor

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. The configuration methods and timings are shown below:

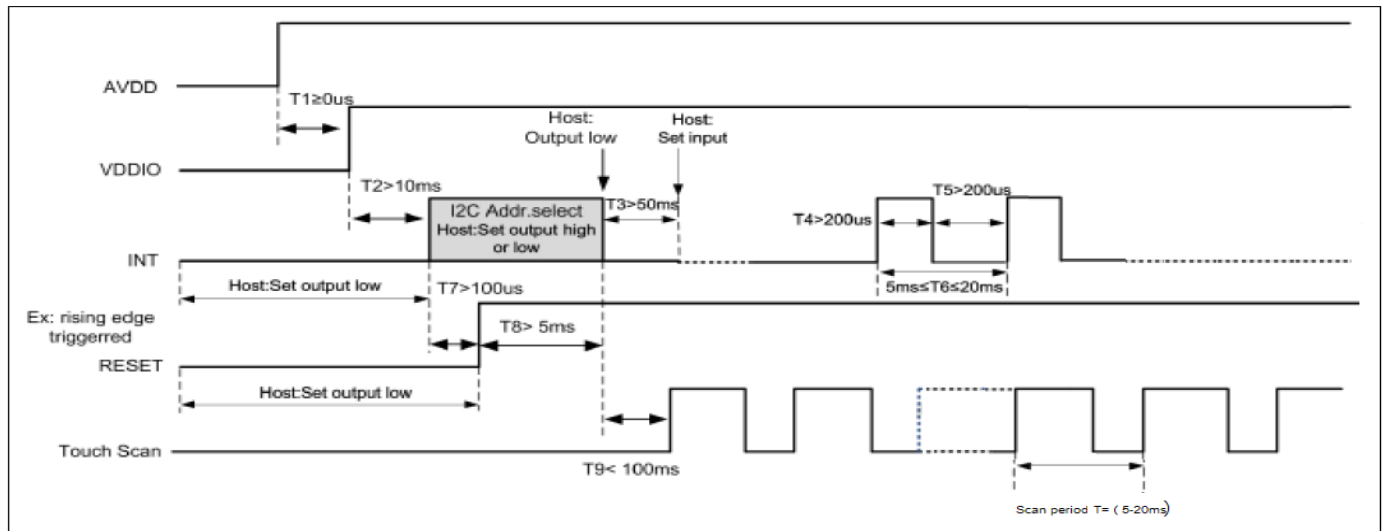


Figure 7.1: I2C Power on Timing

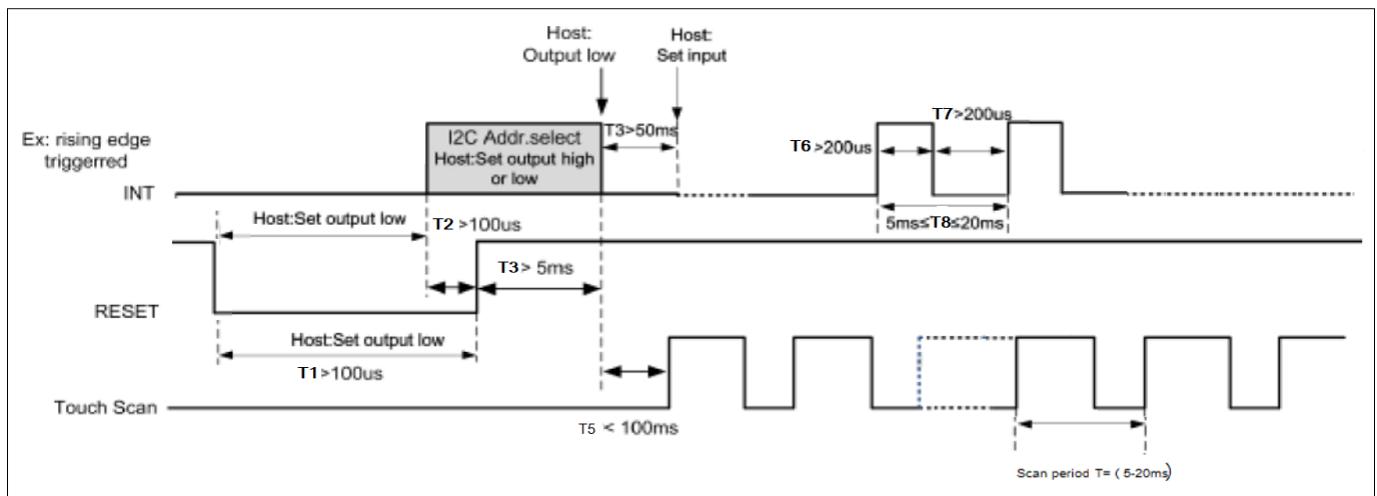


Figure 7.2: I2C Host Resetting Timing

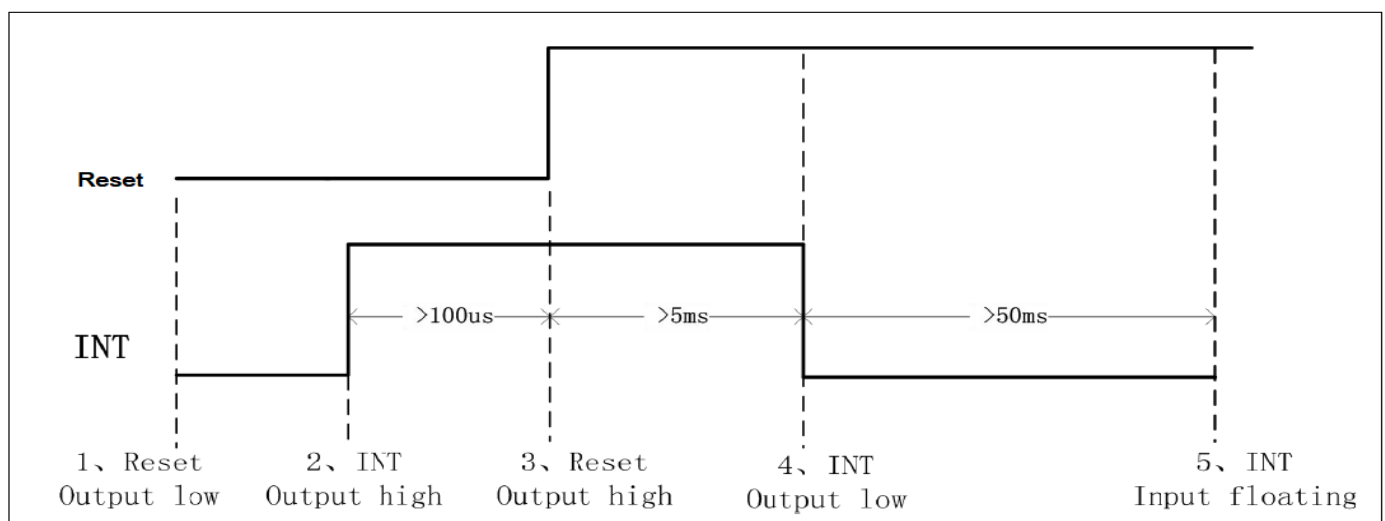


Figure 7.3: Setting Slave Address to 0x28/0x29 Timing

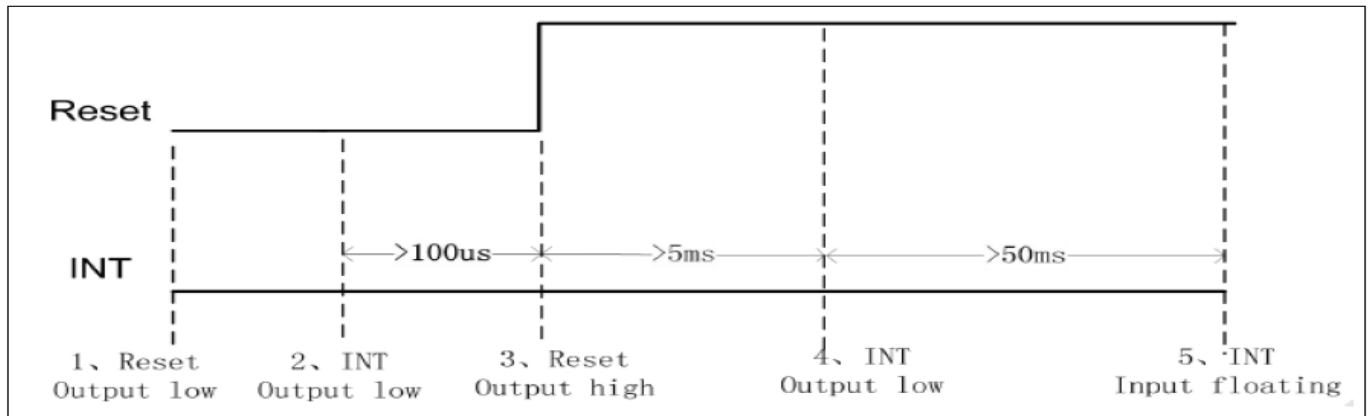


Figure 7.5: Setting Slave Address to 0xBA/0xBB Timing

Data Transmission (ex. 0xBA/0xBB)

Communication is always initiated by the host. Valid start condition is signaled by pulling SDA line from high to low when SCL is high. Data flow or address is transmitted after the start condition.

All slave devices connected to I2C bus should detect the 8-bit address issued after start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely not 0xBA or 0xBB, GT911 will stay in an idle state.

For data bytes on SDA, each of the 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is high. When communication is completed the host will issue the stop condition. Stop condition implies the transition of SDA line from low to high when SCL is high.

Writing Data to GT911

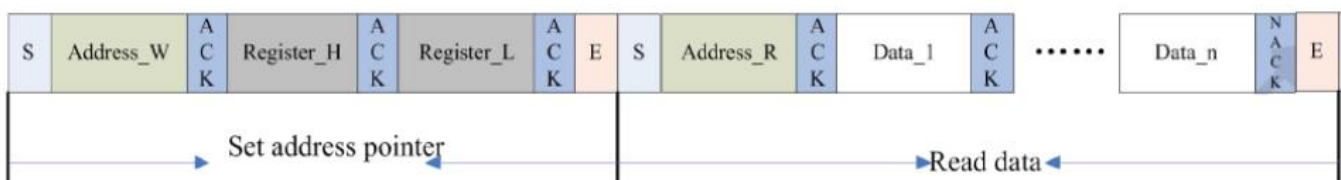
The diagram displays the timing sequence of the host writing data onto GT911. First the host issues a start condition. The host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register)



The location of the register address pointer will automatically add 1 every write operation. When the host needs to perform write operations on a group of registers of continuous addresses it can write continuously. The write operation is terminated when the host issues the stop condition.

Reading Data from GT911

The diagram below is the timing sequence of the host reading data from GT911. The host issues the start condition and sends 0xBA (Address bits and R/W bit; R/W bit as 0 indicates write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.



The host issues the start condition once again and sends 0xBB (read operation). After receiving ACK, the host starts to read the data. GT911 also supports continuous read operation. When receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the "Power ON" condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.