C4H18W500A

Power GaN transistor

Rev. 1 — 24 September 2021

AMPLEON

Product data sheet

1. Product profile

1.1 General description

500 W GaN packaged asymmetric Doherty power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty application demo circuit. V_{DS} = 48 V; I_{Dq} = 350 mA (main), $V_{GS(amp)peak}$ = –4.8 V, unless otherwise specified.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR	$P_{L(5dB)}$
	(MHz)	(mA)	(V)	(dBm)	(dB)	(%)	(dBc)	(dBm)
1-carrier W-CDMA [1]	1805 to 1880	350	48	49.2	15.0	59.0	–31.0	-
pulsed CW [2]	1805 to 1880	350	48	-	-	-	-	57.0

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 10.5 dB at 0.01 % probability on CCDF.

[2] Test signal: pulsed CW; t_p = 30 μs; δ = 35 %.

1.2 Features and benefits

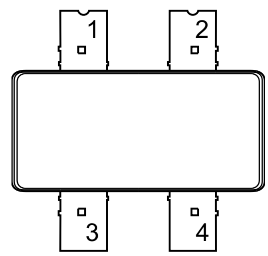
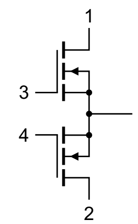
- Excellent digital pre-distortion capability
- High efficiency
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Internally matched for ease of use

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 1800 MHz to 2000 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1273-1	C4H18W500AZ	9349 604 86517	Tray; 20-fold; dry pack	60
	C4H18W500AY	9349 604 86518	TR13; 100-fold; 44 mm; dry pack	100

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	operating	-	52	V
V_{DS}	drain-source voltage	$V_{GS} = -8$ V	-	150	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–15	+2	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–15	+2	V
$I_{GF(amp)main}$	main amplifier forward gate current		-	24	mA
$I_{GF(amp)peak}$	peak amplifier forward gate current		-	40	mA
T_{stg}	storage temperature		–65	+150	°C
T_{ch}	active die channel temperature	[1]	-	275	°C
T_{case}	case temperature	operating [1]	–40	+130	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(s-c)(IR)}$ [1][3]	thermal resistance from active die surface to case by Infrared measurement	V_{DS} = 48 V; I_{Dq} = 250 mA; $V_{GS(amp)peak}$ = –5 V; T_{case} = 80 °C; CW; P_L = 80 W; P_{dis} = 62 W	0.77	K/W
$R_{th(ch-c)(FEA)}$ [2][3][4]	thermal resistance from active die channel to case by Finite Element Analysis	T_{case} = 81 °C; P_{dis} = 65 W	1.44	K/W

[1] Infrared (IR) thermal values are for reference only and cannot be used to determine performance or reliability.

[2] Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

[3] P_{dis} is total Doherty dissipation power which includes main and peak amplifier.

[4] Peak amplifier is assumed to contribute 10 % Doherty dissipation power.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 24 mA	–3.30	–2.65	–2.00	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 480 mA	–3.30	–2.65	–2.00	V
$I_{D(leak)}$	drain leakage current	V_{GS} = –10 V; V_{DS} = 50 V	-	-	5.81	mA
I_{GSS}	gate leakage current	V_{GS} = –8 V; V_{DS} = 0 V	-	-	1.16	mA
Peak device						
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 40 mA	–2.80	–2.15	–1.50	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 800 mA	–2.80	–2.15	–1.50	V
$I_{D(leak)}$	drain leakage current	V_{GS} = –10 V; V_{DS} = 50 V	-	-	9.68	mA
I_{GSS}	gate leakage current	V_{GS} = –8 V; V_{DS} = 0 V	-	-	2.42	mA

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 1807.5 MHz; f_2 = 1877.5 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 250 mA; $V_{GS(amp)peak}$ = –5.0 V (typical); T_{case} = 25 °C; unless otherwise specified; in a Doherty production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 83.2 W	13.6	14.6	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 83.2 W	50.5	56.0	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 83.2 W	-	–16	–8	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 83.2 W	-	–32.0	–28.0	dBc

Table 8. RF characteristics

Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; f = 1880 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 250 mA; $V_{GS(amp)peak}$ = –5.0 V (typical); T_{case} = 25 °C; unless otherwise specified; in a Doherty production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	-	335	410	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The C4H18W500A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 52 V; I_{Dq} = 250 mA; $V_{GS(amp)peak}$ = –5.0 V; P_L = 550 W (pulsed CW; t_p = 100 μs; δ = 10 %); f = 1805 MHz; tested on the Doherty development RF test circuit.

7.2 Impedance information

Table 9. Typical impedance of maximum power and drain efficiency

Measured load-pull data (main device); all data measured on a harmonic impedance non-optimized load-pull fixture; I_{Dq} = 550 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 μs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	P_L [2]	η_D [2]	G_p [2]	AM/PM [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)	(°)
Maximum power load							
1805	4.6 – j11.0	3.3 – j0.8	53.8	240	70.9	15.3	–12
1842	5.0 – j11.8	3.0 – j1.8	53.9	247	65.4	14.7	–9
1880	5.9 – j12.4	3.2 – j2.0	53.9	248	66.3	14.9	–10
1930	7.4 – j13.6	3.0 – j2.1	54.0	250	64.8	14.7	–11
1960	8.7 – j14.1	2.9 – j2.3	54.0	249	64.3	14.8	–11
1990	9.7 – j14.3	2.9 – j2.2	54.0	249	66.2	14.8	–12
Maximum drain efficiency load							
1805	4.6 – j11.0	3.2 + j1.1	52.4	172	77.4	16.4	–21
1842	5.0 – j11.8	2.5 + j1.1	52.0	158	78.6	17.2	–24
1880	5.9 – j12.4	2.6 + j1.0	51.9	154	78.8	17.4	–23
1930	7.4 – j13.6	2.4 + j0.7	52.0	157	77.5	17.1	–27
1960	8.7 – j14.1	2.4 + j0.6	51.9	154	77.7	17.1	–29
1990	9.7 – j14.3	2.4 – j0.2	52.7	186	76.9	16.6	–26

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of maximum power and drain efficiency

Measured load-pull data (peak device); all data measured on a harmonic impedance non-optimized load-pull fixture; I_{Dq} = 780 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 μs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	P_L [2]	η_D [2]	G_p [2]	AM/PM [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)	(°)
Maximum power load							
1805	4.8 – j8.8	1.5 – j1.5	56.3	422	63.0	14.1	–7
1842	5.6 – j9.5	1.5 – j1.5	56.3	424	66.6	14.5	–9
1880	6.8 – j9.7	1.6 – j1.7	56.3	426	66.9	14.5	–9
1930	9.3 – j8.4	1.7 – j1.9	56.0	402	67.1	15.1	–9
1960	10.3 – j7.7	1.7 – j2.1	55.9	392	66.3	15.2	–9

Table 10. Typical impedance of maximum power and drain efficiency *…continued*

Measured load-pull data (peak device); all data measured on a harmonic impedance non-optimized load-pull fixture; I_{Dq} = 780 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 µs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	P_L [2]	η_D [2]	G_p [2]	AM/PM [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)	(°)
1990	10.9 – j6.9	1.6 – j2.0	55.9	387	68.4	15.4	–11
Maximum drain efficiency load							
1805	4.8 – j8.8	1.9 – j0.2	54.8	300	72.6	16.0	–19
1842	5.6 – j9.5	1.4 + j0.0	53.7	234	72.7	16.3	–26
1880	6.8 – j9.7	1.4 – j0.1	53.8	238	73.3	16.2	–25
1930	9.3 – j8.4	1.7 – j0.9	54.8	305	74.6	16.7	–21
1960	10.3 – j7.7	1.7 – j1.0	54.7	292	74.2	16.6	–20
1990	10.9 – j6.9	1.6 – j1.0	54.1	259	73.9	16.8	–22

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

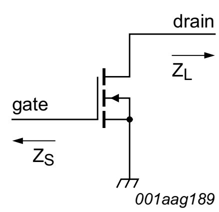


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main device at 1 : 1 load

Measured load-pull data (main device); I_{Dq} = 550 mA; V_{DS} = 48 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]	AM/PM [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)	(°)
1805	4.6 – j11.0	3.3 – j0.4	228	73.5	15.6	–15
1842	5.0 – j11.8	3.1 – j0.5	233	75.2	15.8	–14
1880	5.9 – j12.4	3.1 – j0.7	234	75.1	15.9	–14
1930	7.4 – j13.6	2.8 – j0.8	238	74.2	15.8	–17
1960	8.7 – j14.1	2.6 – j0.9	236	74.6	15.9	–17
1990	9.7 – j14.3	3.0 – j1.3	234	72.1	15.7	–17

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 12. Typical impedance of main device at 1 : 1.5 load

Measured load-pull data (main device); I_{Dq} = 550 mA; V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [3]	G_p [3]	AM/PM [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)	(°)
1805	4.6 – j11.0	2.2 + j2.1	112	66.9	19.1	–31
1842	5.0 – j11.8	2.3 + j2.0	112	68.4	19.2	–28
1880	5.9 – j12.4	2.1+ j1.6	116	67.8	19.3	–27
1930	7.4 – j13.6	2.0 + j1.4	110	67.6	19.5	–33
1960	8.7 – j14.1	2.0 + j1.1	113	66.7	19.5	–34
1990	9.7 – j14.3	1.9 + j0.7	121	65.8	19.3	–33

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

[3] At P_L = 83.2 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data (peak device); I_{Dq} = 780 mA; V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]	AM/PM [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)	(°)
1805	4.8 – j8.8	1.6 – j1.1	404	67.9	14.7	–11
1842	5.6 – j9.5	1.6 – j1.2	405	69.1	14.9	–12
1880	6.8 – j9.7	1.6 – j1.4	405	69.8	14.9	–12
1930	9.3 – j8.4	1.5 – j1.4	376	72.2	15.7	–13
1960	10.3 – j7.7	1.5 – j1.5	365	71.6	15.7	–13
1990	10.9 – j6.9	1.5 – j1.7	362	71.0	15.8	–15

[1] Z_S and Z_L defined in Figure 1.

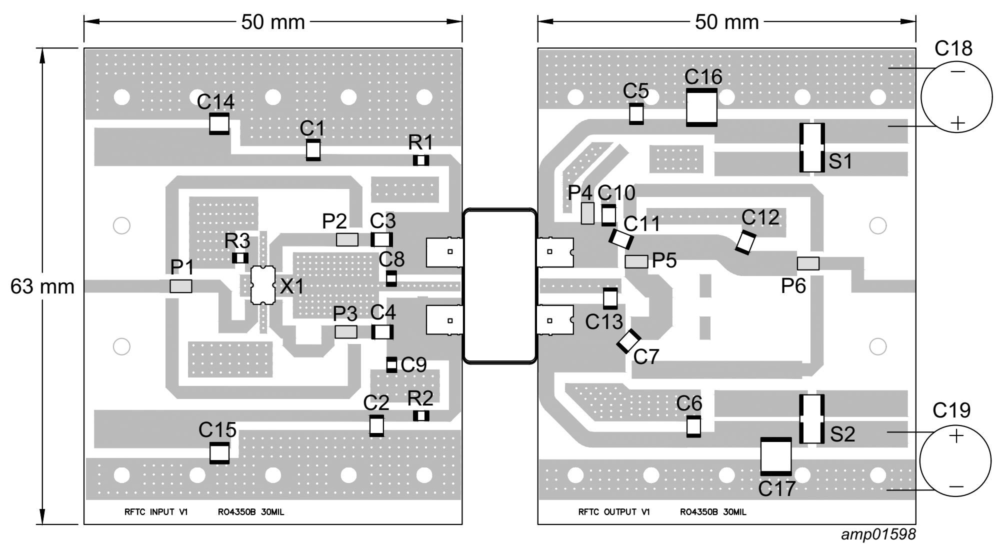
[2] At 3 dB gain compression.

Table 14. Typical off-state impedance of peak device

Measured under the following conditions: V_{DS} = 48 V; V_{GS} = –5.0 V.

f	Z_{off}
(MHz)	(Ω)
1805	0.2 – j1.6
1842	0.2 – j1.4
1880	0.2 – j1.2
1930	0.2 – j1.0
1960	0.2 – j0.8
1990	0.2 – j0.6

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B; ε_r = 3.66; thickness = 0.762 mm; thickness copper plating = 35 μm. See Table 15 for a list of components.

Fig 2. Component layout for Doherty development RF test circuit

Table 15. List of components

See Figure 2 for component layout.

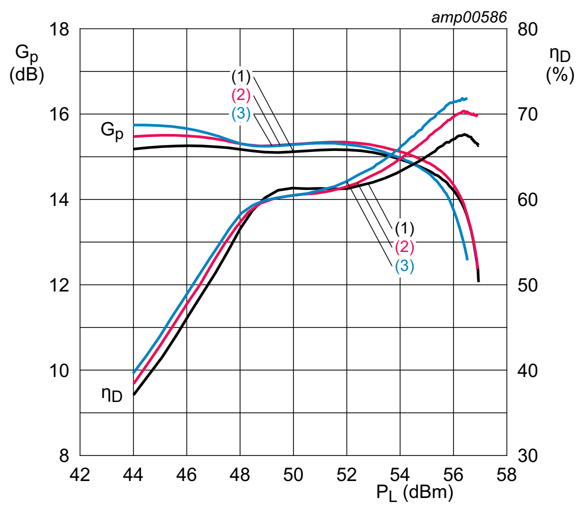
Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6, C7	multilayer ceramic chip capacitor	22 pF	ATC 800B
C8	multilayer ceramic chip capacitor	0.5 pF	ATC 600F
C9	multilayer ceramic chip capacitor	1.6 pF	ATC 600F
C10	multilayer ceramic chip capacitor	1.4 pF	ATC 800B
C11	multilayer ceramic chip capacitor	3.3 pF	ATC 800B
C12	multilayer ceramic chip capacitor	0.5 pF	ATC 800B
C13	multilayer ceramic chip capacitor	2.4 pF	ATC 800B
C14, C15	multilayer ceramic chip capacitor	1 μF, 100 V	Murata GRM31CR72A105KA01L
C16, C17	multilayer ceramic chip capacitor	10 μF, 100 V	Murata KRM55QR72A106KH01L
C18, C19	electrolytic capacitor	1000 μF, 100 V	
P1, P2, P3, P4, P5, P6	copper foil		
R1, R2	resistor	9.1 Ω	SMD 0805
R3	resistor	51 Ω	SMD 0805
S1, S2	four terminal high precision current sense resistor		Ohmite: LVK25 (1224) or of same quality
X1	hybrid coupler	2 dB, 90°	Anaren: X3C20F1-02S

7.5 Graphical data

All data are measured on the Doherty development RF test circuit.

7.5.1 Pulsed CW

t_p = 100 μs; δ = 10 %; V_{DS} = 48 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = –5.0 V.

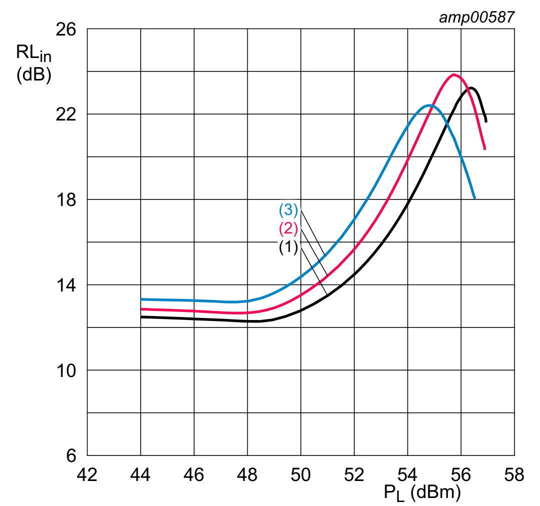


(1) f = 1805 MHz

(2) f = 1842 MHz

(3) f = 1880 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



(1) f = 1805 MHz

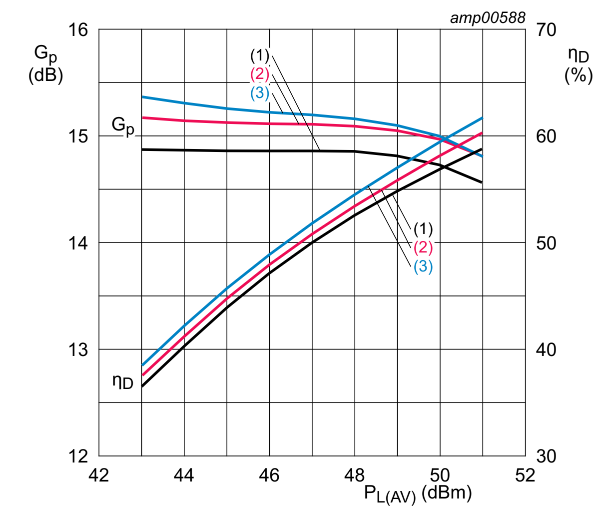
(2) f = 1842 MHz

(3) f = 1880 MHz

Fig 4. Input return loss as a function of output power; typical values

7.5.2 1-Carrier W-CDMA

PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; V_{DS} = 48 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = –5.0 V.

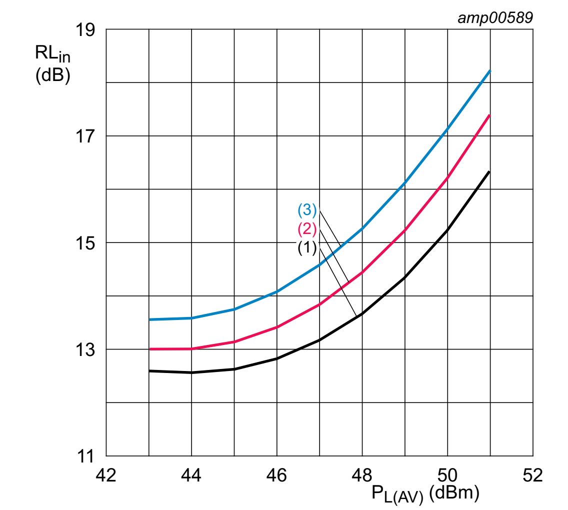


(1) f = 1807.5 MHz

(2) f = 1842 MHz

(3) f = 1877.5 MHz

Fig 5. Power gain and drain efficiency as function of average output power; typical values

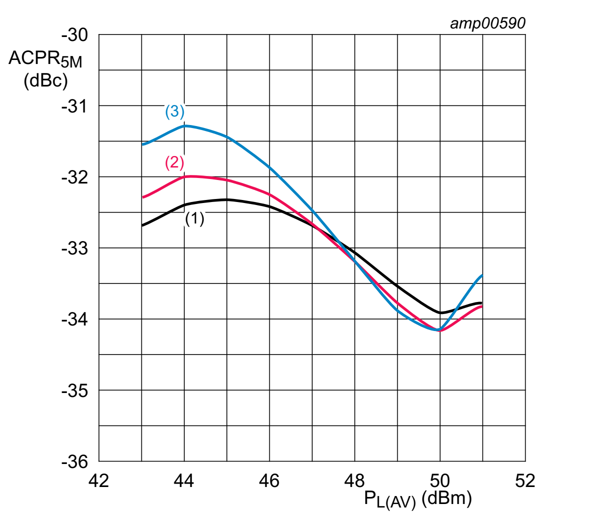


(1) f = 1807.5 MHz

(2) f = 1842 MHz

(3) f = 1877.5 MHz

Fig 6. Input return loss as a function of average output power; typical values

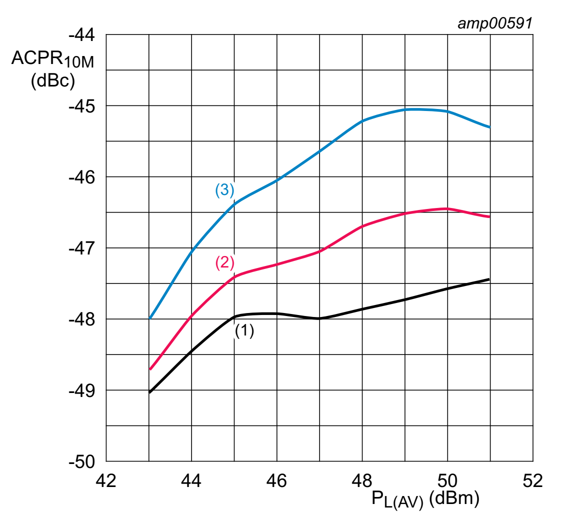


(1) f = 1807.5 MHz

(2) f = 1842 MHz

(3) f = 1877.5 MHz

Fig 7. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values



(1) f = 1807.5 MHz

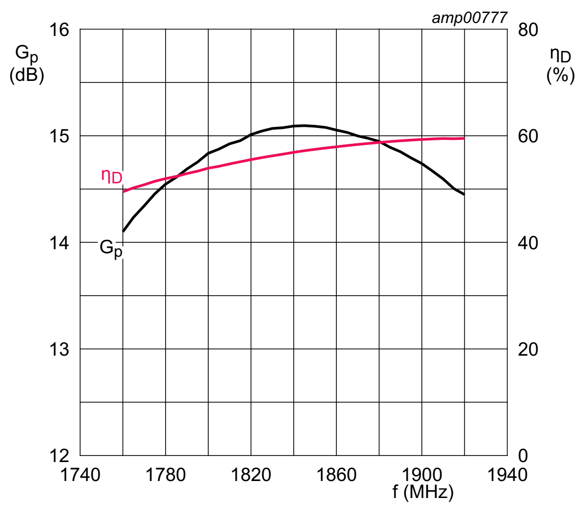
(2) f = 1842 MHz

(3) f = 1877.5 MHz

Fig 8. Adjacent channel power ratio (10 MHz) as a function of average output power; typical values

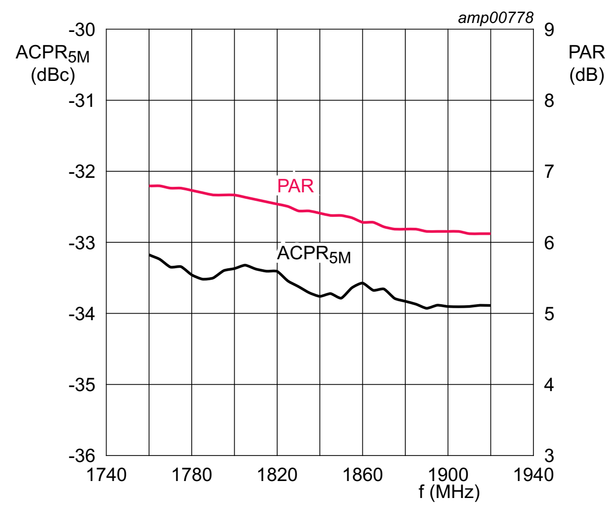
7.5.3 Broadband performance

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; V_{DS} = 48 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = –5.0 V.



$P_{L(AV)}$ = 49.2 dBm.

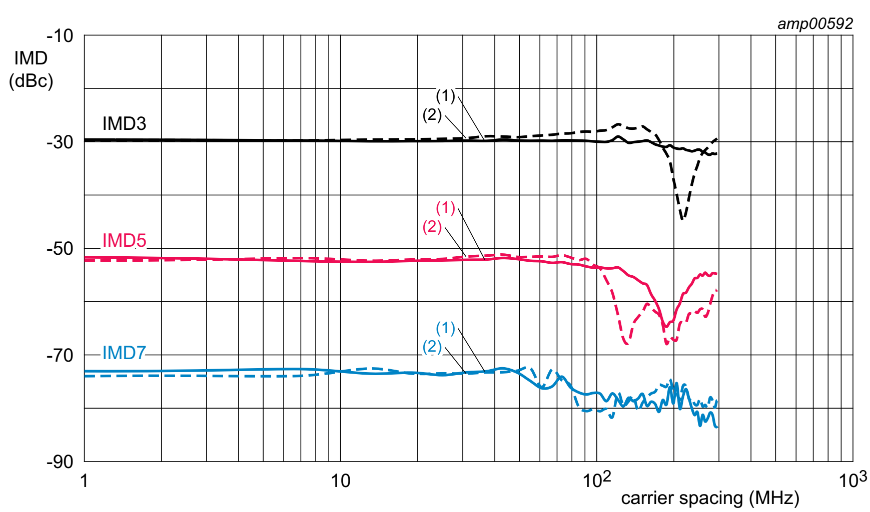
Fig 9. Power gain and drain efficiency as function of frequency; typical values



$P_{L(AV)}$ = 49.2 dBm.

Fig 10. Adjacent channel power ratio (5 MHz) and peak-to-average ratio as a function of frequency; typical values

7.5.4 2-Tone VBW



V_{DS} = 48 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = –5.0 V; f_c = 1842 MHz; P_L = 27 dBm.

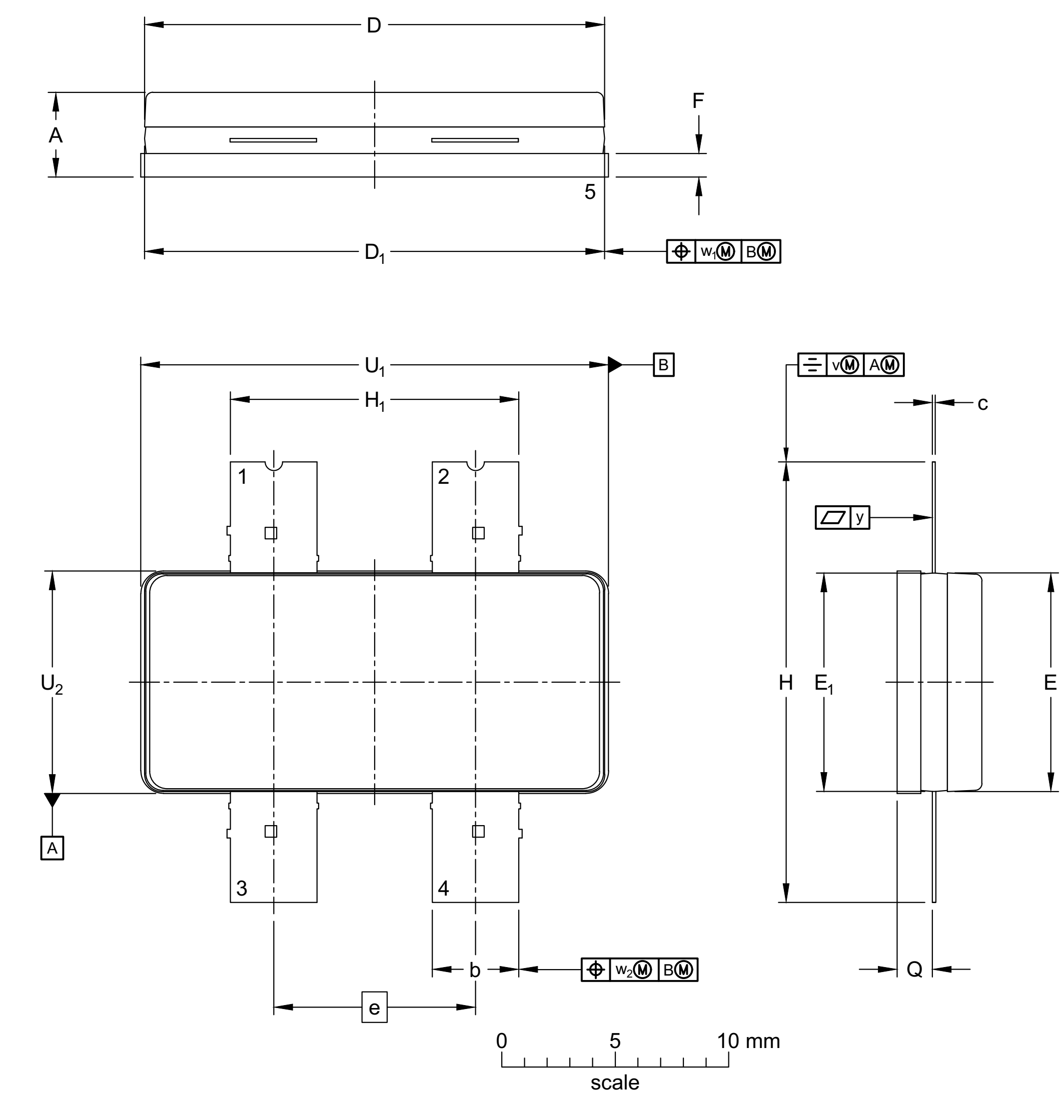
(1) IMD low

(2) IMD high

Fig 11. VBW capability on the Doherty Development RF test circuit

8. Package outline

Air cavity plastic earless flanged package; 4 leads SOT1273-1



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
mm	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Note:
1. Dimension Q is measured at 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1273-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1273-1						17-01-12

Fig 12. Package outline SOT1273-1

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1B [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 1B is granted to any part that passes after exposure to an ESD pulse of 500 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
GaN	Gallium Nitride
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
PM	Phase Modulation
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
C4H18W500A v.1	20210924	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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