

## N-channel 650 V, 0.039 $\Omega$ typ., 63 A MDmesh™ M2 Power MOSFET in a TO-247 package

Datasheet - production data

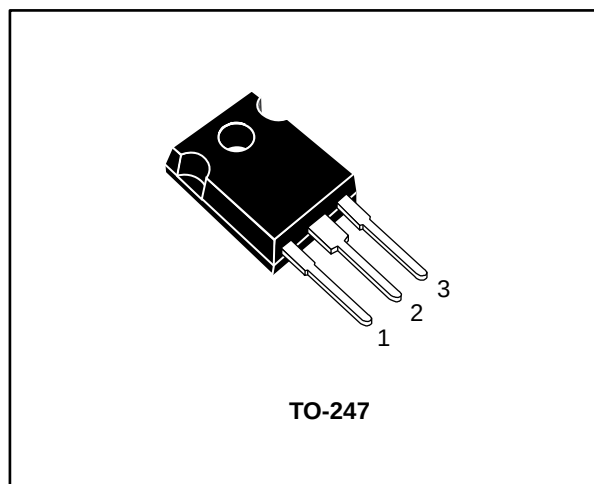
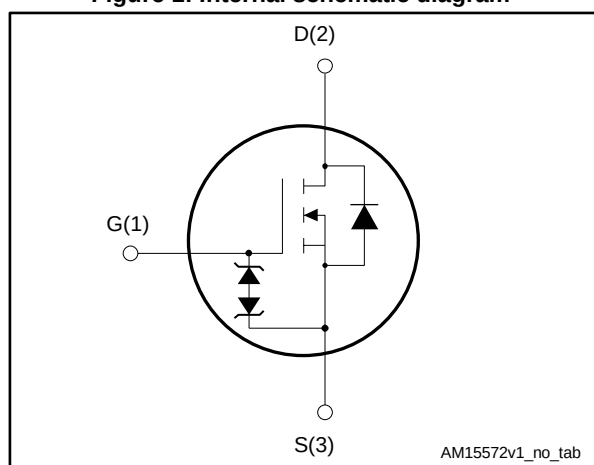


Figure 1: Internal schematic diagram



### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STW70N65M2 | 650 V           | 0.046 $\Omega$           | 63 A           |

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|---------|-----------|
| STW70N65M2 | 70N65M2 | TO-247  | Tube      |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol         | Parameter                                           | Value       | Unit |
|----------------|-----------------------------------------------------|-------------|------|
| $V_{GS}$       | Gate-source voltage                                 | $\pm 25$    | V    |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ °C}$  | 63          | A    |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ °C}$ | 40          | A    |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                              | 252         | A    |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ °C}$           | 446         | W    |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                   | 15          | V/ns |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                           | 50          | V/ns |
| $T_{stg}$      | Storage temperature range                           | - 55 to 150 | °C   |
| $T_j$          | Operating junction temperature range                |             |      |

**Notes:**

<sup>(1)</sup> Pulse width limited by safe operating area.

<sup>(2)</sup>  $I_{SD} \leq 63\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$

<sup>(3)</sup>  $V_{DS} \leq 520\text{ V}$

Table 3: Thermal data

| Symbol         | Parameter                               | Value | Unit |
|----------------|-----------------------------------------|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case max    | 0.28  | °C/W |
| $R_{thj-amb}$  | Thermal resistance junction-ambient max | 50    | °C/W |

Table 4: Avalanche characteristics

| Symbol   | Parameter                                                                                                | Value | Unit |
|----------|----------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetetive or not repetetive (pulse width limited by $T_{jmax}$ )                     | 4     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 3500  | mJ   |

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

Table 5: On/off states

| Symbol        | Parameter                         | Test conditions                                                                                         | Min. | Typ.  | Max.    | Unit          |
|---------------|-----------------------------------|---------------------------------------------------------------------------------------------------------|------|-------|---------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                             | 650  |       |         | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$                                                         |      |       | 1       | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ ,<br>$T_C = 125\text{ }^{\circ}\text{C}$ <sup>(1)</sup> |      |       | 100     | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                                      |      |       | $\pm 5$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                                      | 2    | 3     | 4       | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 31.5\text{ A}$                                                          |      | 0.039 | 0.046   | $\Omega$      |

**Notes:**

<sup>(1)</sup> Defined by design, not subject to production test.

Table 6: Dynamic

| Symbol                              | Parameter                     | Test conditions                                                                                                                                     | Min. | Typ. | Max. | Unit     |
|-------------------------------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$                           | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0\text{ V}$                                                                             | -    | 5140 | -    | pF       |
| $C_{oss}$                           | Output capacitance            |                                                                                                                                                     | -    | 208  | -    | pF       |
| $C_{rss}$                           | Reverse transfer capacitance  |                                                                                                                                                     | -    | 2.9  | -    | pF       |
| $C_{oss\text{ eq.}}$ <sup>(1)</sup> | Equivalent output capacitance | $V_{DS} = 0\text{ V to } 520\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                      | -    | 520  | -    | pF       |
| $R_G$                               | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                             | -    | 3    | -    | $\Omega$ |
| $Q_g$                               | Total gate charge             | $V_{DD} = 520\text{ V}$ , $I_D = 63\text{ A}$ ,<br>$V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> ) | -    | 117  | -    | nC       |
| $Q_{gs}$                            | Gate-source charge            |                                                                                                                                                     | -    | 21.5 | -    | nC       |
| $Q_{gd}$                            | Gate-drain charge             |                                                                                                                                                     | -    | 51   | -    | nC       |

**Notes:**

<sup>(1)</sup>  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 7: Switching times

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                                                       | Min. | Typ. | Max. | Unit |
|--------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 325\text{ V}$ , $I_D = 31.5\text{ A}$<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 24   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                                                       | -    | 22   | -    | ns   |
| $t_{d(off)}$ | Turn-off-delay time |                                                                                                                                                                                                                                                       | -    | 134  | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                                                       | -    | 11   | -    | ns   |

Table 8: Source drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                                       | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                                       | -    |      | 63   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                                       | -    |      | 252  | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 63\text{ A}$                                                                                                                                                                                        | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 63\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )                                     | -    | 584  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                       | -    | 14.5 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                       | -    | 50.5 |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 63\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 725  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                                       | -    | 20   |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                                       | -    | 55.5 |      | A             |

**Notes:**

<sup>(1)</sup> Pulse width is limited by safe operating area

<sup>(2)</sup> Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

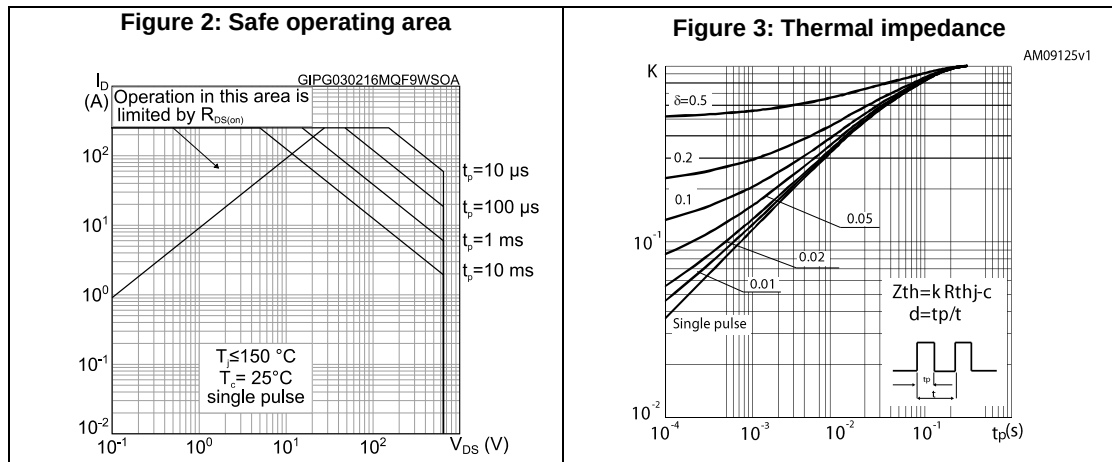


Figure 3: Thermal impedance

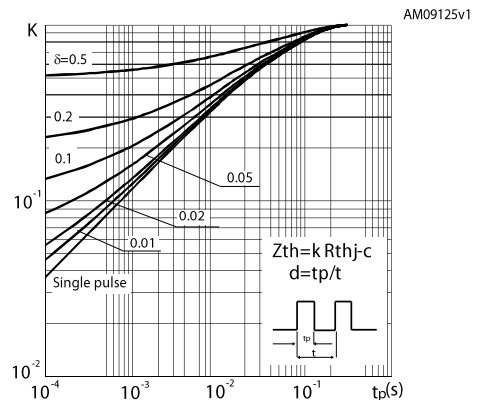


Figure 4: Output characteristics

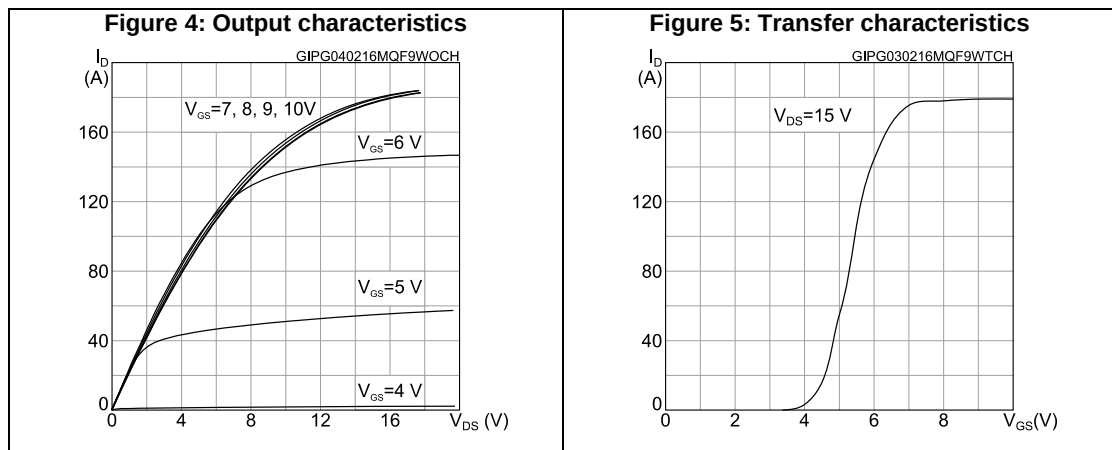


Figure 5: Transfer characteristics

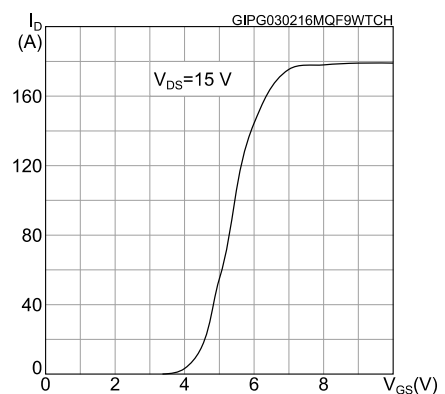


Figure 6: Gate charge vs. gate-source voltage

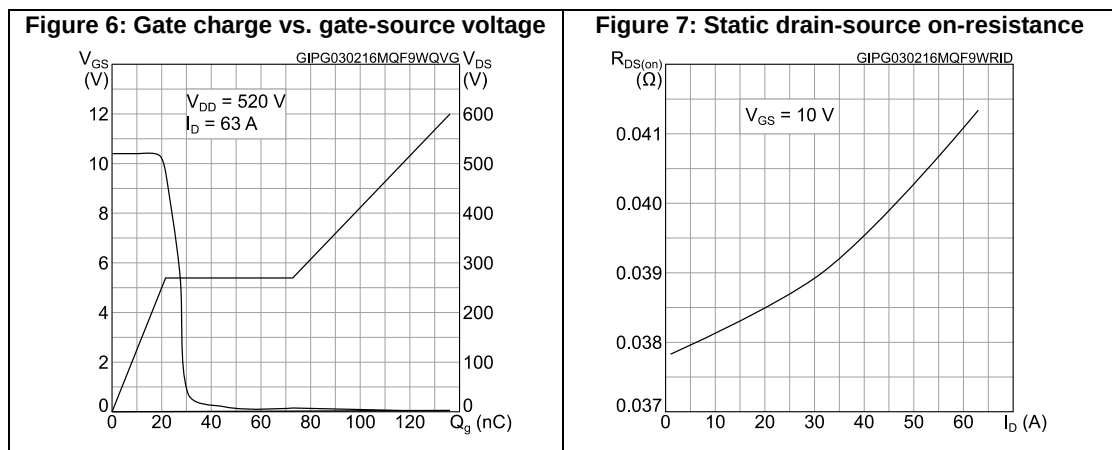


Figure 7: Static drain-source on-resistance

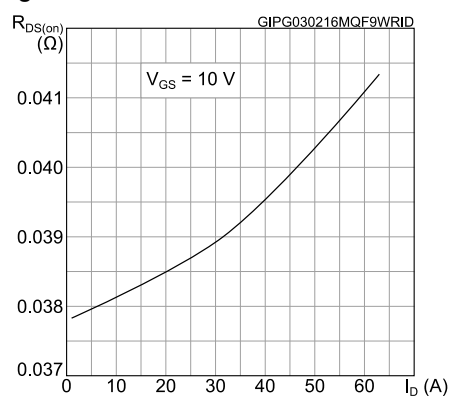


Figure 8: Capacitance variations

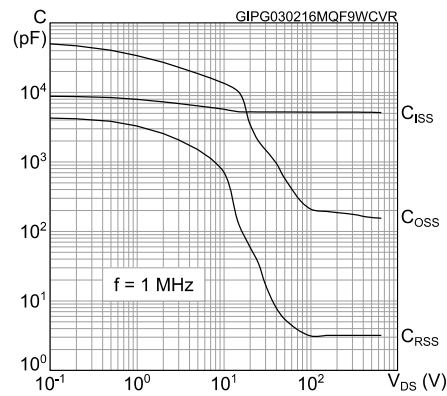


Figure 9: Normalized gate threshold voltage vs temperature

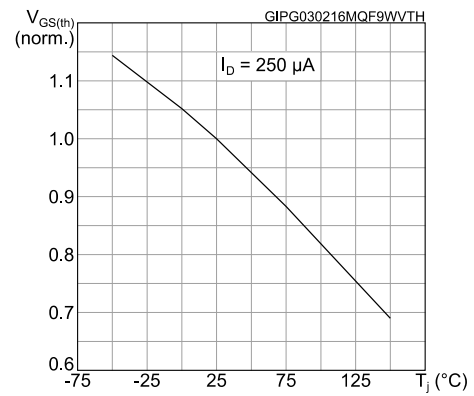


Figure 10: Normalized on-resistance vs temperature

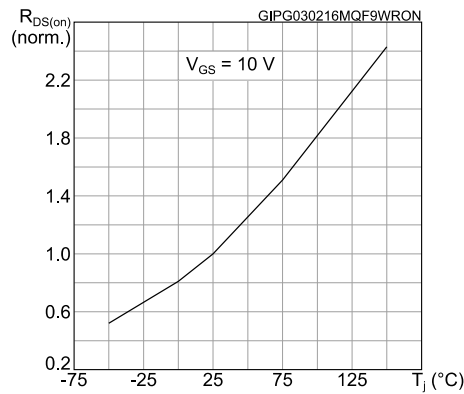
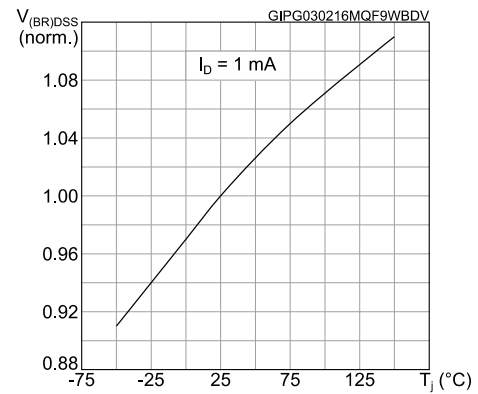
Figure 11: Normalized  $V_{(BR)DSS}$  vs temperature

Figure 12: Output capacitance stored energy

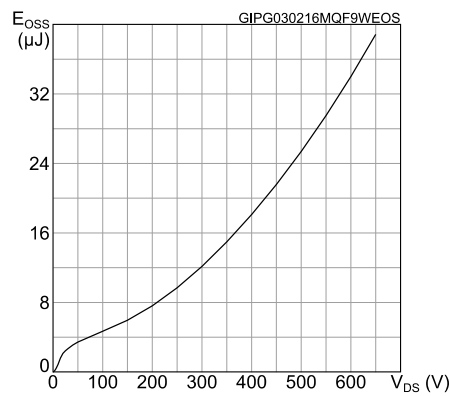
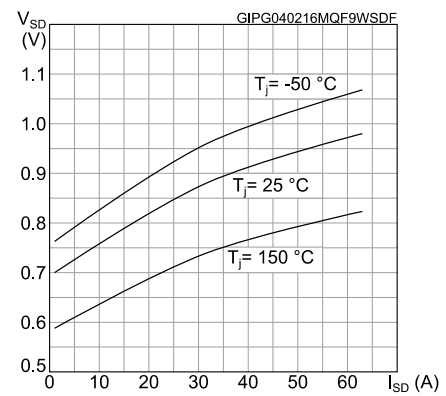
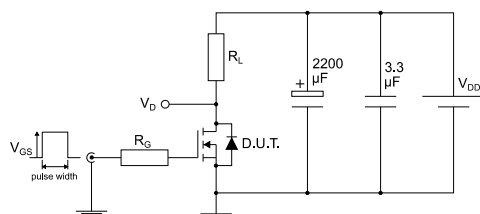


Figure 13: Source-drain diode forward characteristics



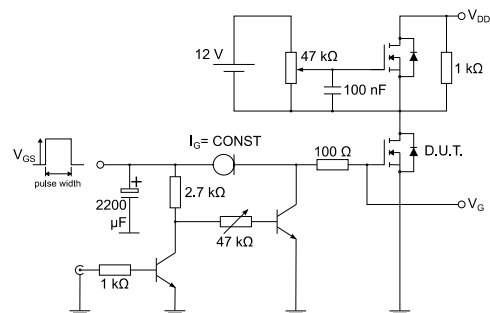
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



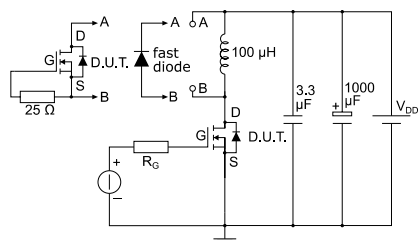
AM01468v1

**Figure 15: Test circuit for gate charge behavior**



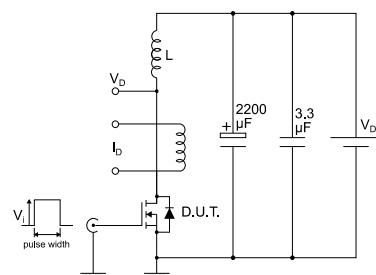
AM01469v1

**Figure 16: Test circuit for inductive load switching and diode recovery times**



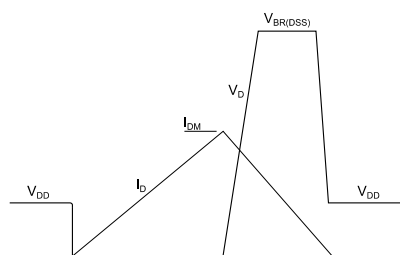
AM01470v1

**Figure 17: Unclamped inductive load test circuit**



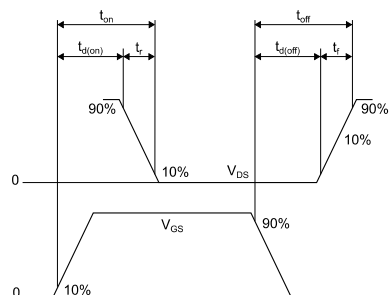
AM01471v1

**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-247 package information

Figure 20: TO-247 package outline

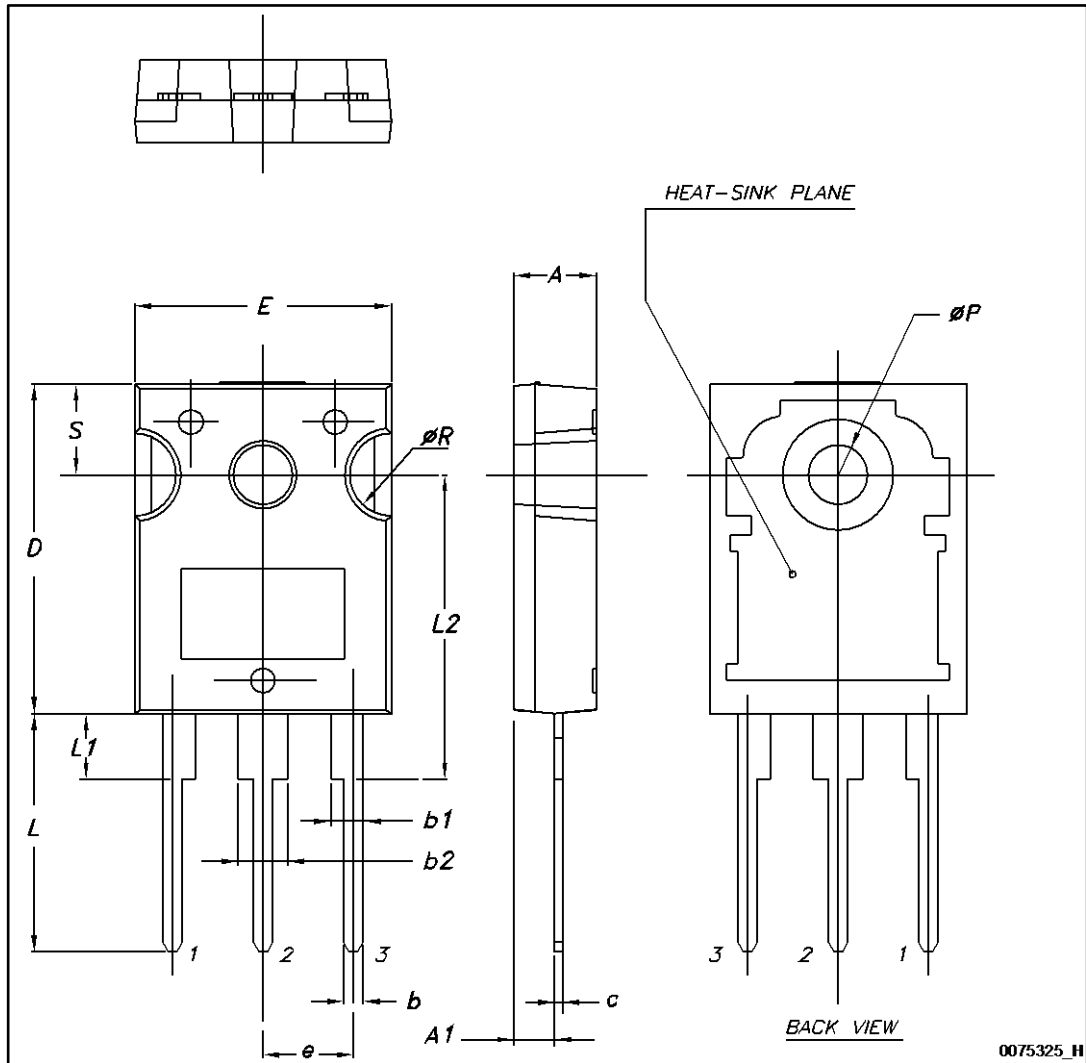


Table 9: TO-247 package mechanical data

| Dim. | mm.   |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.85  |       | 5.15  |
| A1   | 2.20  |       | 2.60  |
| b    | 1.0   |       | 1.40  |
| b1   | 2.0   |       | 2.40  |
| b2   | 3.0   |       | 3.40  |
| c    | 0.40  |       | 0.80  |
| D    | 19.85 |       | 20.15 |
| E    | 15.45 |       | 15.75 |
| e    | 5.30  | 5.45  | 5.60  |
| L    | 14.20 |       | 14.80 |
| L1   | 3.70  |       | 4.30  |
| L2   |       | 18.50 |       |
| ØP   | 3.55  |       | 3.65  |
| ØR   | 4.50  |       | 5.50  |
| S    | 5.30  | 5.50  | 5.70  |

## 5 Revision history

Table 10: Document revision history

| Date        | Revision | Changes        |
|-------------|----------|----------------|
| 04-Feb-2016 | 1        | First release. |

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