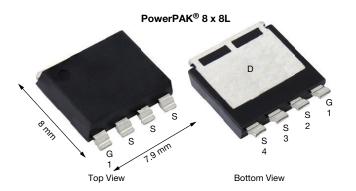


Vishay Siliconix

AUTOMOTIVE GRADE

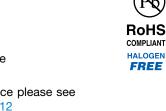
# Automotive N-Channel 30 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	30			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.00052			
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0007			
I <sub>D</sub> (A)	445			
Configuration	Single			
Package	PowerPAK 8 x 8L			

#### **FEATURES**

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>q</sub> and UIS tested
- Thin 1.6 mm package
- · Very low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



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N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SQJQ130EL (for detailed order number please see <a href="https://www.vishay.com/doc?79776">www.vishay.com/doc?79776</a> )

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	30	V	
Gate-source voltage		V <sub>GS</sub>	± 20	V	
Continuous drain current	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	445		
	T <sub>C</sub> = 125 °C		445		
Continuous source current (diode conduction)		I <sub>S</sub>	545	Α	
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	445		
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	86		
Single pulse avalanche energy	L = U.1 IIII	E <sub>AS</sub>	374	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C	В	600	W	
	T <sub>C</sub> = 125 °C	P <sub>D</sub>	200		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>d</sup>			260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount c	$R_{thJA}$	44	°C/W	
Junction-to-case (drain)		R <sub>thJC</sub>	0.25	C/VV	

#### Notes

- a. Package limited
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static		<u> </u>		l	•	•	
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0$ , $I_D = 250 \mu A$		30	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	- V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	2.0	2.5	V
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero gate voltage drain current		$V_{GS} = 0 V$	$V_{GS} = 0 \text{ V}$ $V_{DS} = 30 \text{ V}$ -		-	1	
	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 30 V, T <sub>J</sub> = 125 °C	-	-	200	μΑ
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 30 V, T <sub>J</sub> = 175 °C	-	-	330	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	100	-	-	Α
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.00045	0.00052	Ω
Drain actures on state registeres 3	B	V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 20 A	-	0.0006	0.0007	
Drain-source on-state resistance a	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0008	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0009	
Forward transconductance b	9fs	$V_{DS}$	= 15 V, I <sub>D</sub> = 60 A	-	360	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		V <sub>DS</sub> = 25 V, f = 1 MHz	-	16 675	23 345	pF
Output capacitance	Coss	V <sub>GS</sub> = 0 V		-	6850	9560	
Reverse transfer capacitance	C <sub>rss</sub>			-	715	1000	
Total gate charge c	$Q_g$		10 V V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	-	310	455	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		-	53	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>				56	-	1
Gate resistance	$R_g$	f = 1 MHz		0.9	1.9	2.9	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	22	33	
Rise time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 15 \text{ V, } R_L = 0.5 \Omega$ $I_D \cong 30 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega$		-	30	45	ns
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	109	164	
Fall time <sup>c</sup>	t <sub>f</sub>			-	57	86	
Source-Drain Diode Ratings and Cha	aracteristics b						
	t <sub>rr</sub>			-	40	-	
Reverse recovery time			-	44	-	ns	
	t <sub>b</sub>	V <sub>DD</sub> = 24 V, I <sub>FM</sub> = 20 A, di/dt = 100 A/μs		-	83		166
Reverse recovery charge	Q <sub>rr</sub>			-	156	312	nC
Reverse recovery current	I <sub>RM</sub>	1		-	-	3.4	Α
Pulsed current a	I <sub>SM</sub>			-	-	1600	Α
		I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0			1		

#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

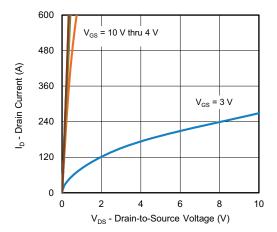


Fig. 1 - Output Characteristics

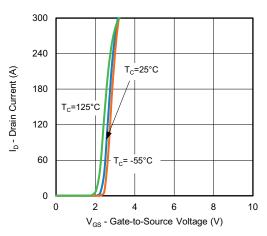


Fig. 2 - Transfer Characteristics

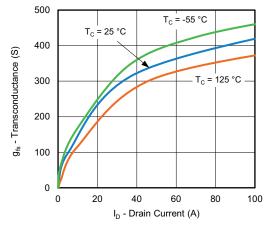


Fig. 3 - Transconductance

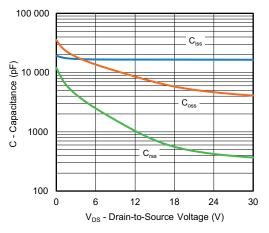


Fig. 4 - Capacitance

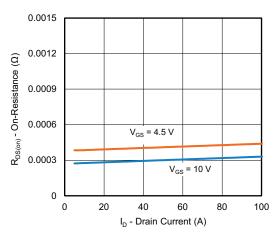


Fig. 5 - On-Resistance vs. Drain Current

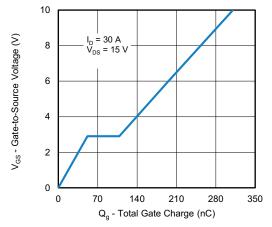


Fig. 6 - Gate Charge



## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

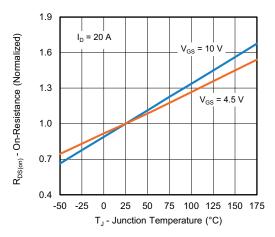


Fig. 7 - On-Resistance vs. Junction Temperature

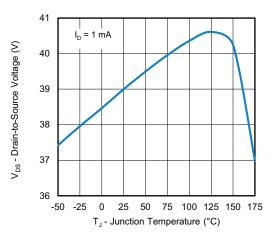


Fig. 8 - Drain Source Breakdown vs. Junction Temperature

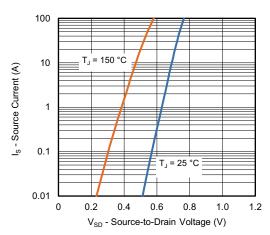


Fig. 9 - Source Drain Diode Forward Voltage

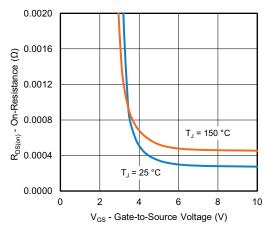


Fig. 10 - On-Resistance vs. Gate-to-Source Voltage

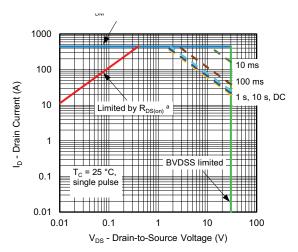


Fig. 11 - Safe Operating Area

#### Note

a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)

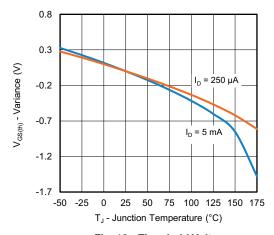


Fig. 12 - Threshold Voltage

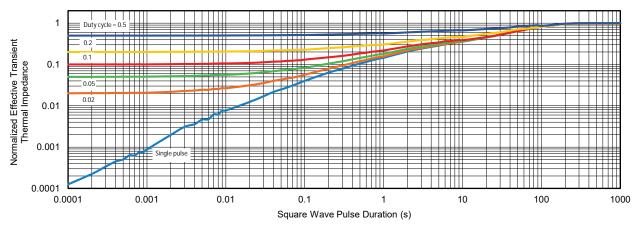


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

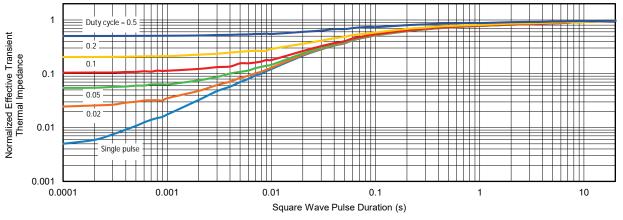


Fig. 14 - Normalized Thermal Transient Impedance, Junction-to-Case

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