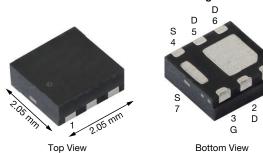


www.vishay.com

Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® SC-70W-6L Single



Marking Code: QTXXXX

PRODUCT SUMMARY				
V _{DS} (V)	40			
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.0144			
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0200			
I _D (A)	9			
Configuration	Single			

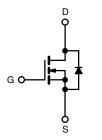
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R_a and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





HALOGEN FREE



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA440CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATIN	GS ($T_C = 25$ °C, unles	s otherwise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	40		
Gate-source voltage		V _{GS} ± 20		V	
Continuous drain current ^a	T _C = 25 °C		9		
	T _C = 125 °C	I _D	9		
Continuous source current (diode conduction) ^a		Is	9	Α	
Pulsed drain current ^a		I _{DM}	36		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	12.5		
Single pulse avalanche energy	L = U.1 Min	E _{AS}	7.81	mJ	
Maximum power dissipation	T _C = 25 °C	D	13.6	W	
	T _C = 125 °C	P_{D}	4.5		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) d, e			260	T.	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount c	R _{thJA}	90	°C/W	
Junction-to-case (drain)		R _{thJC}	11	C/W	

Notes

- a. Package limited
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- c. When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$		1.2	1.7	2.2	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero gate voltage drain current		$V_{GS} = 0 V$	$V_{DS} = 40 \text{ V}$	-	-	1	μΑ
	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	250	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 \text{ V}$	8	-	-	Α
Drain-source on-state resistance a		V _{GS} = 10 V	I _D = 5 A	-	0.0116	0.0144	Ω
	Б	V _{GS} = 10 V	I _D = 5 A, T _J = 125 °C	-	-	0.0224	
	R _{DS(on)}	V _{GS} = 10 V	I _D = 5 A, T _J = 175 °C	-	-	0.0263	
		V _{GS} = 4.5 V	$I_D = 4 A$	-	0.0161	0.0200	1
Forward transconductance b	9 _{fs}	V _{DS}	= 15 V, I _D = 5 A	-	28	-	S
Dynamic ^b							•
Input capacitance	C _{iss}			-	608	880	pF
Output capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	167	245	
Reverse transfer capacitance	C _{rss}			-	20	29	
Total gate charge ^c	Qg			-	11.4	17.5	nC
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_{D} = 5 \text{ A}$	-	2.1	-	
Gate-drain charge ^c	Q _{gd}			-	2.0	-	
Gate resistance	R_g	f = 1 MHz		1.2	2.4	3.6	Ω
Turn-on delay time ^c	t _{d(on)}	$V_{DD} = 20 \text{ V, } R_L = 4 \Omega$ $I_D \cong 5 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega$		-	8	12	ns
Rise time ^c	t _r			-	4	6	
Turn-off delay time ^c	t _{d(off)}			-	17	26	
Fall time ^c	t _f			-	3	5	
Source-Drain Diode Ratings and Charact	eristics ^b						
Pulsed current a	I _{SM}			-	-	9	Α
Forward voltage	V_{SD}	I _F = 5 A, V _{GS} = 0 V		-	0.81	1.2	V
Body diode reverse recovery time	t _{rr}			-	15	30	ns
Body diode reverse recovery charge	Q _{rr}	I _F = 2 A, di/dt = 100 A/μs		-	7	14	nC
Reverse recovery fall time	ta			-	8	-	
Reverse recovery rise time	t _b			-	7	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}	1		_	-0.8	-	Α

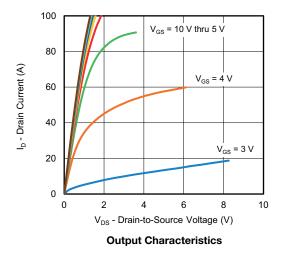
Notes

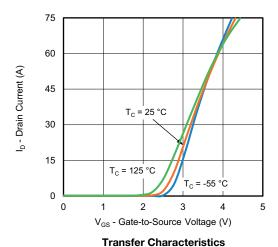
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

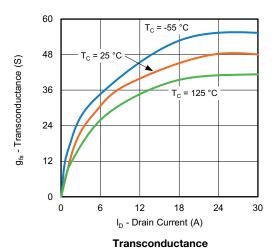
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

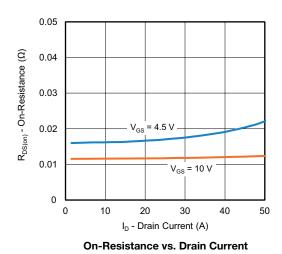


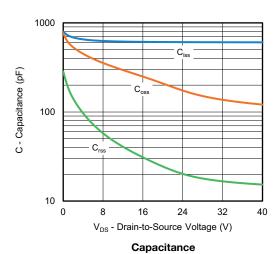
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

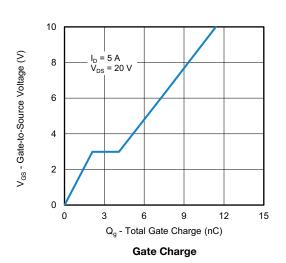






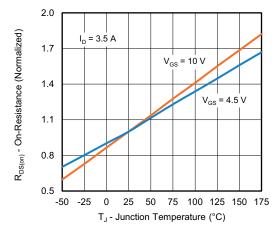




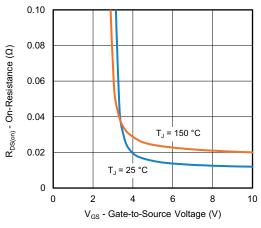




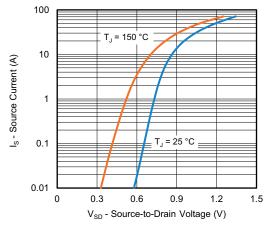
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



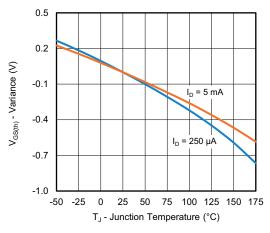
On-Resistance vs. Junction Temperature



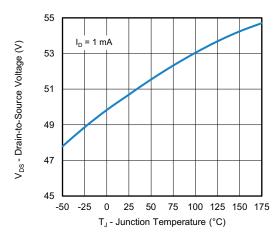
On-Resistance vs. Gate-to-Source Voltage



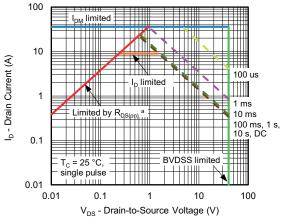
Source Drain Diode Forward Voltage



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



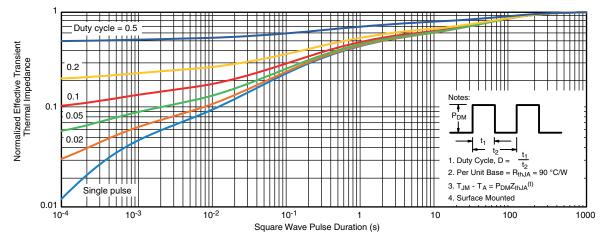
Safe Operating Area

Note

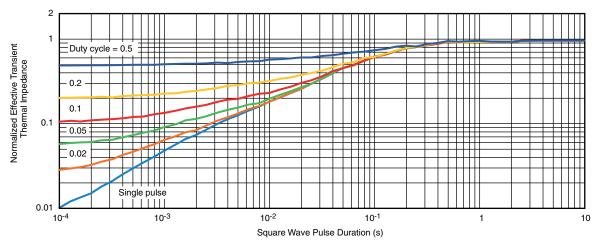
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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