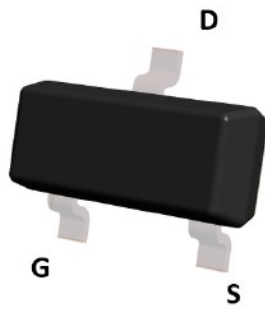


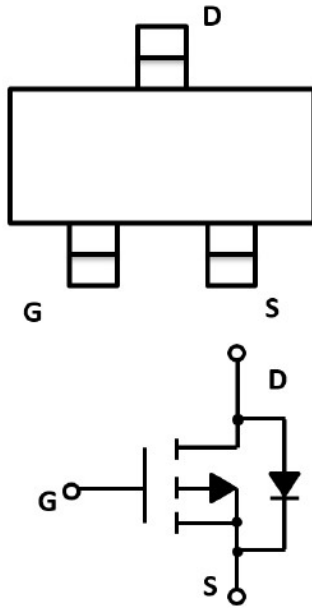


P-Channel Enhancement Mode Field Effect Transistor



Top View

SOT-23



Product Summary

- V_{DS} -30V
- I_D -4.4A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <55mohm
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <66mohm
- $R_{DS(ON)}$ (at $V_{GS}=-2.5V$) <94mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Battery protection
- Power management
- Load switch

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	± 12	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	-4.4	A
	$T_A=70^\circ\text{C}$		-3.5	
Pulsed Drain Current ^A		I_{DM}	-27	A
Total Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.2	W
	$T_A=70^\circ\text{C}$		0.8	
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	104	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3401A	F2	3401.	3000	30000	120000	7" reel



YJL3401A

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V,V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =± 12V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.6	-0.9	-1.4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-4.4A		40	55	mΩ
		V _{GS} =-4.5V, I _D =-4A		47	66	
		V _{GS} =-2.5V, I _D =-2A		60	94	
Diode Forward Voltage	V _{SD}	I _S =-4.4A,V _{GS} =0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V,V _{GS} =0V,f=1MHZ		1040		pF
Output Capacitance	C _{oss}			80		
Reverse Transfer Capacitance	C _{rss}			68		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V,V _{DS} =-15V,I _D =-4.4A		22		nC
Gate-Source Charge	Q _{gs}			3.28		
Gate-Drain Charge	Q _{gd}			2.11		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DS} =-15V, I _D =4.4A R _{GEN} =3Ω		4.4		
Turn-on Rise Time	t _r			26		
Turn-off Delay Time	t _{D(off)}			49.2		
Turn-off fall Time	t _f			42.8		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

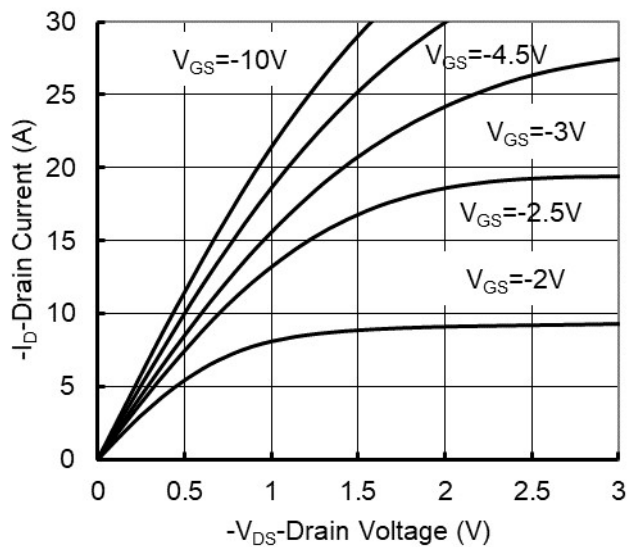


Figure1. Output Characteristics

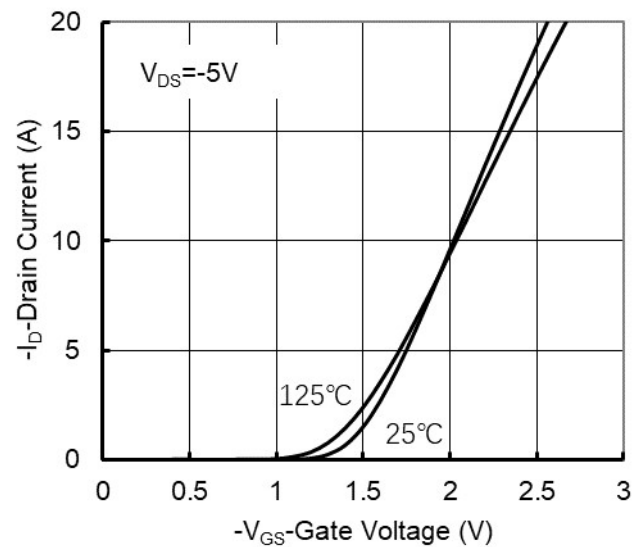


Figure2. Transfer Characteristics

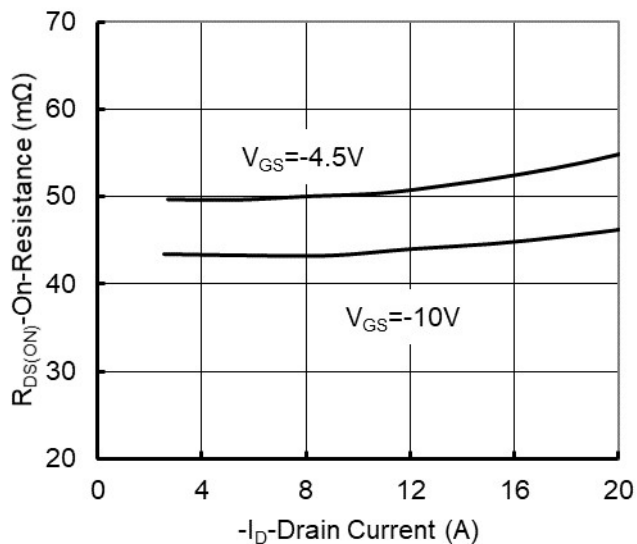


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

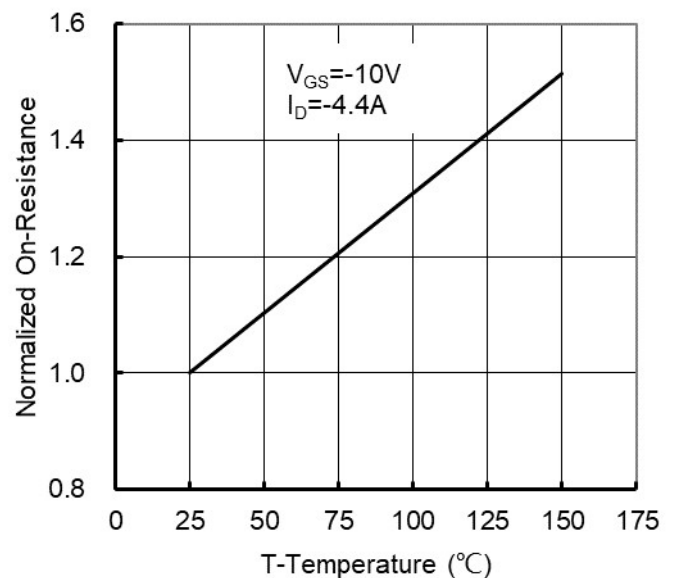


Figure 4: On-Resistance vs. Junction Temperature

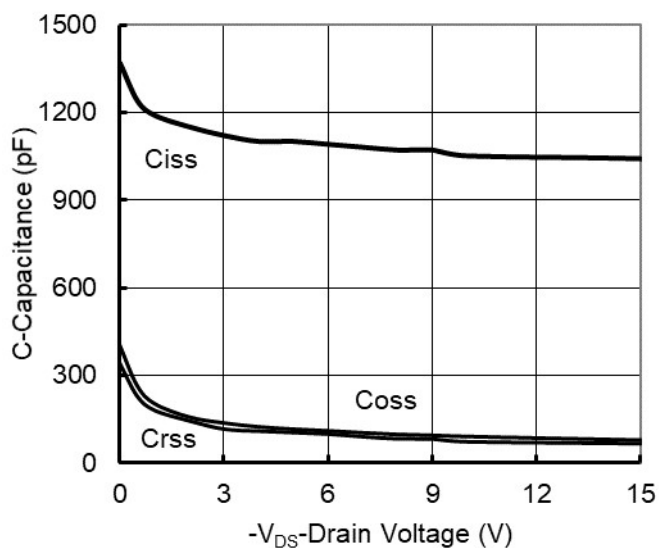


Figure5. Capacitance Characteristics

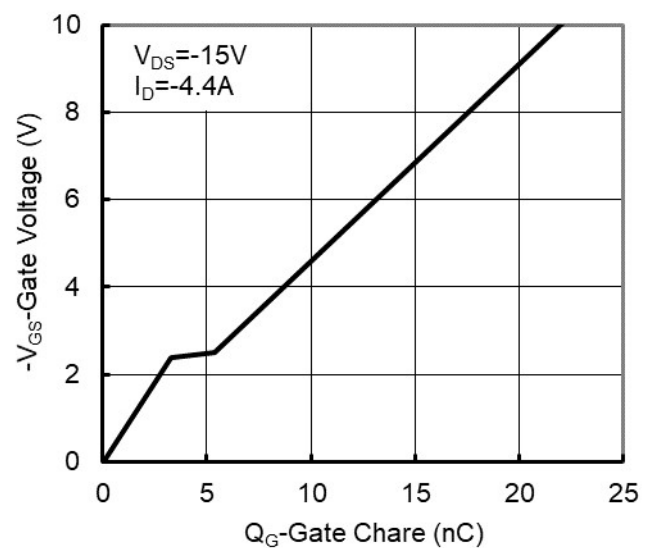


Figure6. Gate Charge

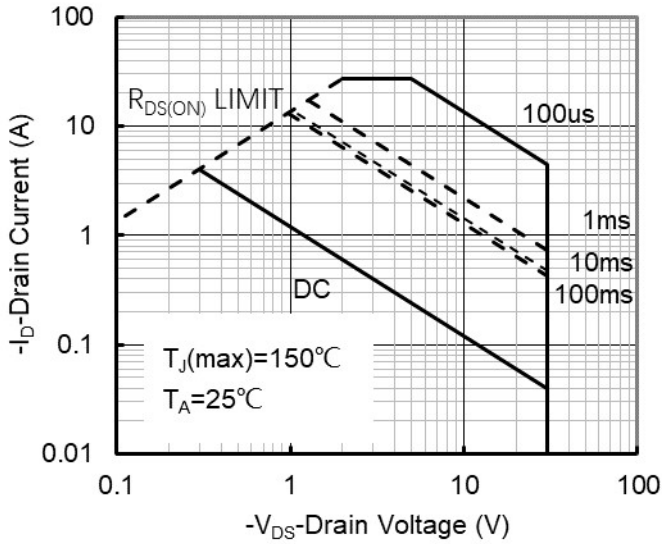


Figure7. Safe Operation Area

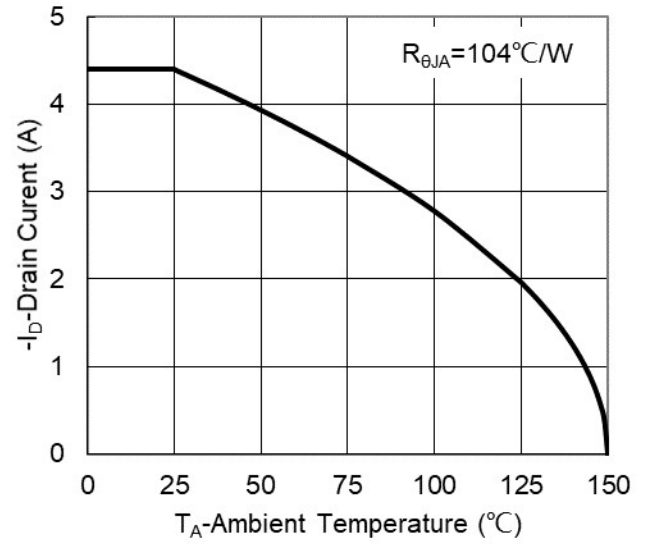


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

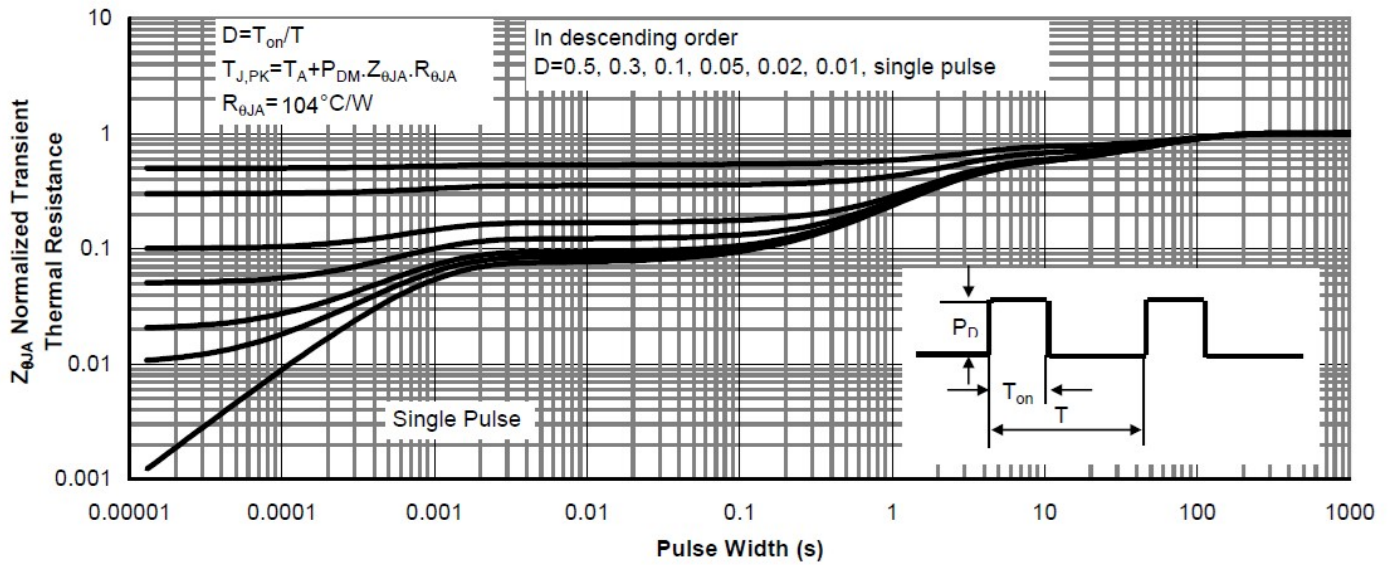
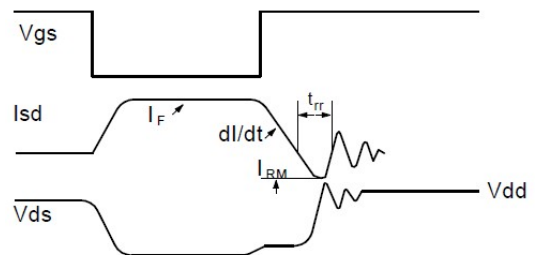


Figure9. Normalized Maximum Transient Thermal Impedance



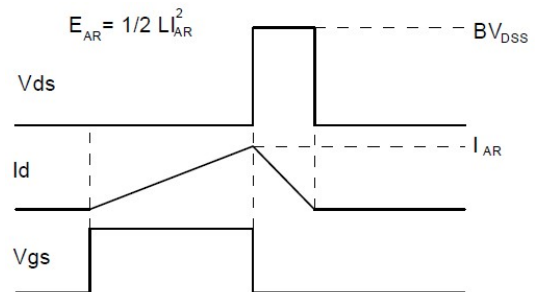
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



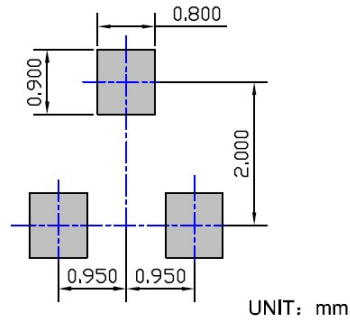
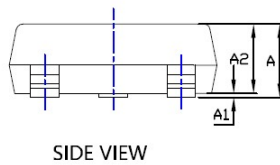
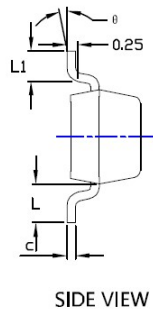
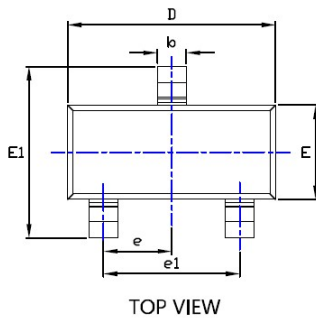
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



■ SOT-23 Package Information



SYMBOL	DIMENSIONS			DIMENSIONS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.035	---	0.045	0.900	---	1.150
A1	0.000	---	0.004	0.000	---	0.100
A2	0.035	0.038	0.041	0.900	0.975	1.050
b	0.012	0.016	0.020	0.300	0.400	0.500
c	0.004	---	0.008	0.100	---	0.200
D	0.110	0.114	0.118	2.800	2.900	3.000
E	0.047	0.051	0.055	1.200	1.300	1.400
E1	0.089	0.094	0.100	2.250	2.400	2.550
e	0.037TYP			0.950TYP		
e1	0.071	0.075	0.079	1.800	1.900	2.000
L	0.022REF			0.550REF		
L1	0.012	0.016	0.200	0.300	0.400	0.500
s	0*	---	8*	0*	---	8*

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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