



BUK9Y13-60EL

Single N-channel 60 V, 7.9 mOhm logic level MOSFET in LFPK56 using Enhanced SOA technology

20 April 2022

Product data sheet

1. General description

Single, logic level, N-channel MOSFET in LFPK56 using Application specific (ASFET) Enhanced SOA technology. This product has been designed and qualified to AEC-Q101 for use in linear mode in airbag applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Enhanced SOA technology for improved linear mode performance
- LFPK copper clip package technology:
 - High robustness and current handling capability
 - Gull wing leads for easy AOI inspection and exceptional board level reliability

3. Applications

- 12 V automotive systems
- Airbag squib voltage regulator MOSFET

4. Quick reference data

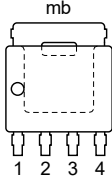
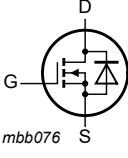
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	60	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	90	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	147	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 13		4.4	6.3	7.9	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 20\text{ A}$; $V_{DS} = 48\text{ V}$; $V_{GS} = 4.5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 15 ; Fig. 16		-	11.7	23.3	nC

[1] 90 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 <i>mbb076</i>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y13-60EL	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y13-60EL	91360EL

8. Limiting values

Table 5. Limiting values

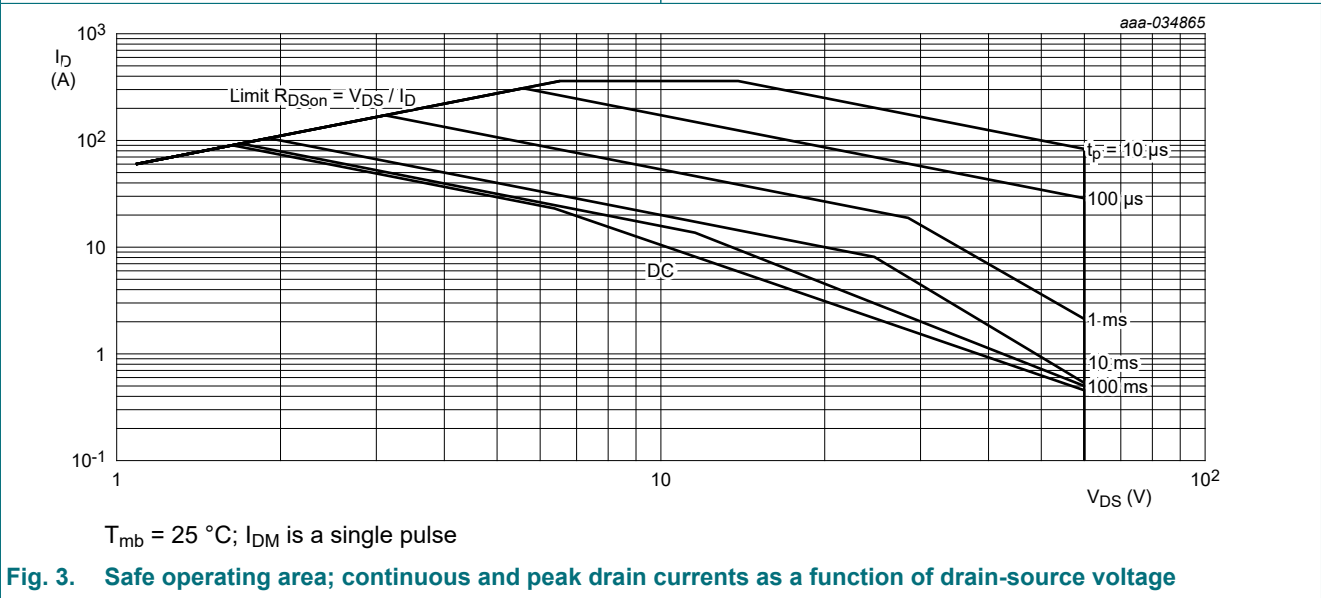
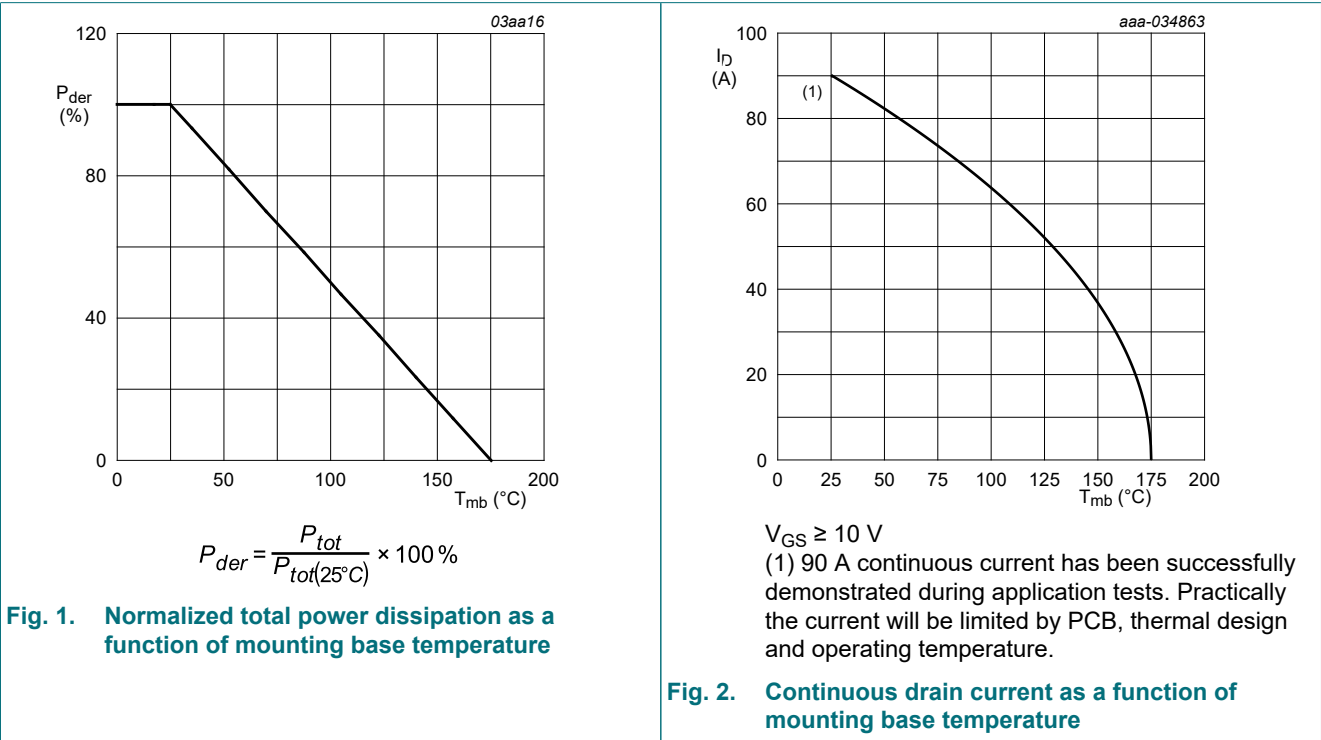
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	60	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$		-10	10	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	147	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	90	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	64	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3; Fig. 4		-	361	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	90	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	361	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 49.7\text{ A}$; $V_{sup} \leq 60\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 62\text{ }\mu\text{s}$; Fig. 5	[2] [3]	-	127	mJ

Single N-channel 60 V, 7.9 mOhm logic level MOSFET in LPAK56 using Enhanced SOA technology

Symbol	Parameter	Conditions		Min	Max	Unit
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 60 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 5	[2] [3] [4]	-	49.7	A

- [1] 90 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Protected by 100% test.



Single N-channel 60 V, 7.9 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

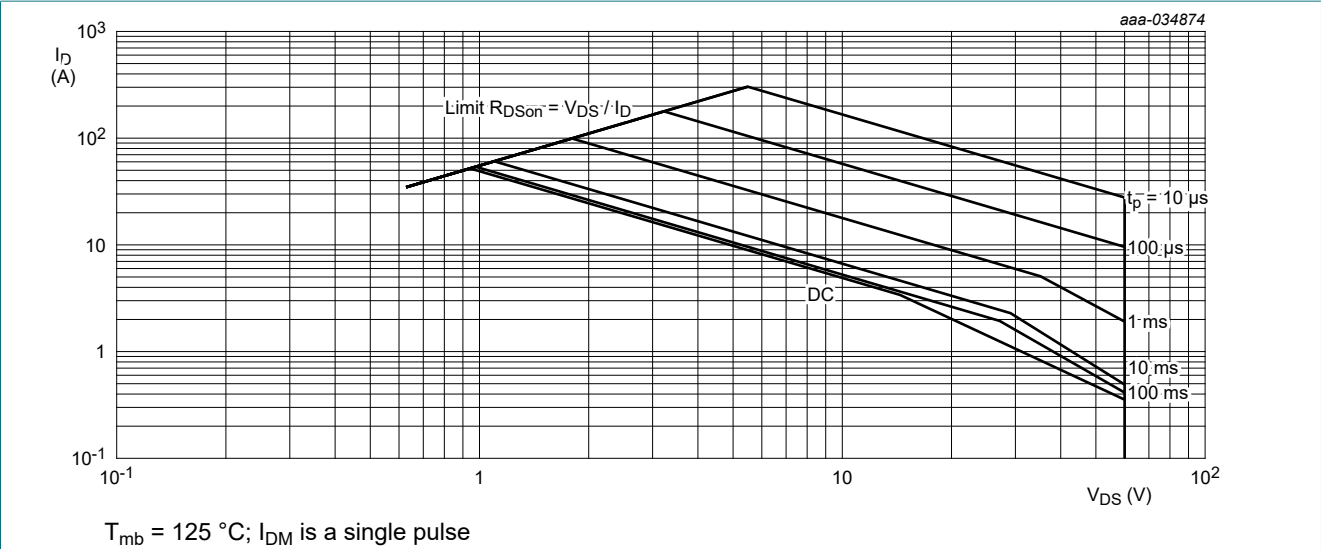


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

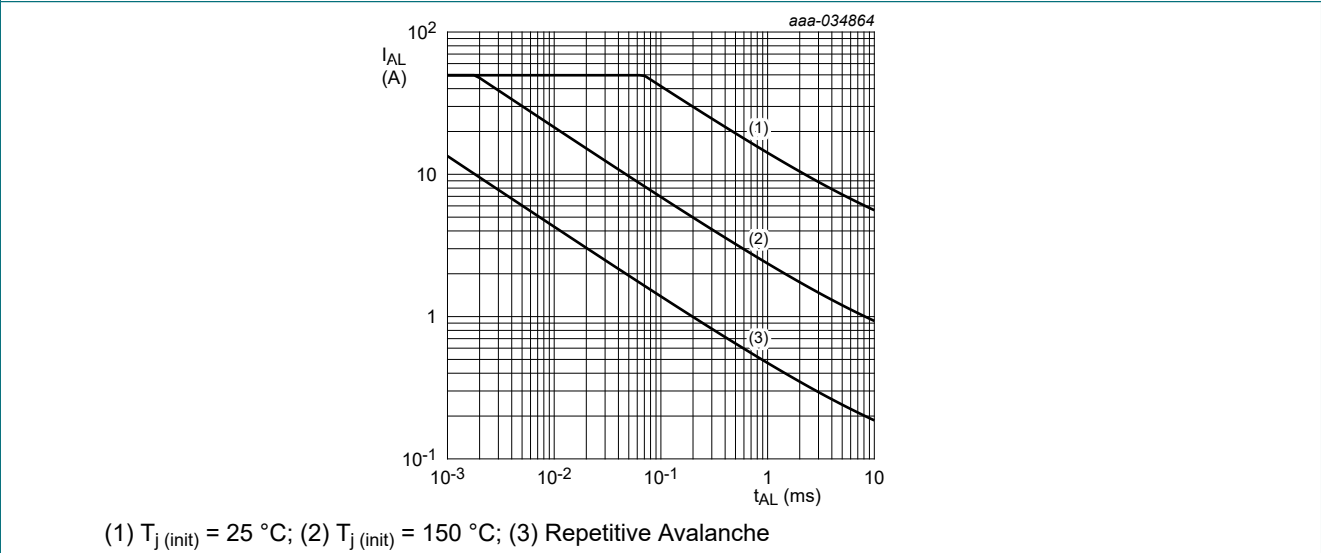


Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	0.92	1.02	K/W

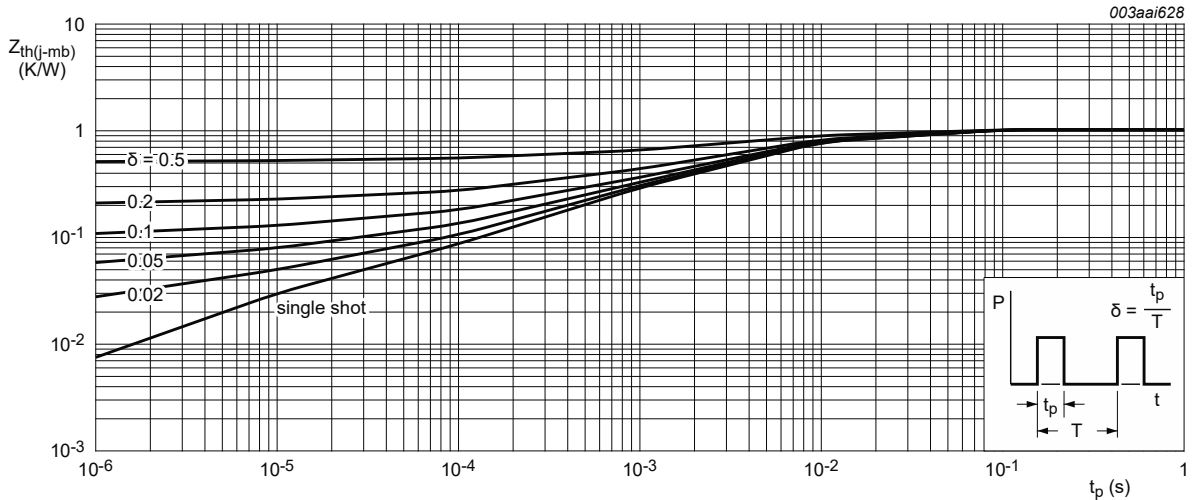


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	60	66	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -40 ^\circ C$	-	61.9	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	54	61	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = 25 ^\circ C$; Fig. 11 ; Fig. 12	1.4	1.78	2.1	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = -55 ^\circ C$; Fig. 12	-	-	2.45	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = 175 ^\circ C$; Fig. 12	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	0.015	1	μA
		$V_{DS} = 60 V$; $V_{GS} = 0 V$; $T_j = 175 ^\circ C$	-	54	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 20 A$; $T_j = 25 ^\circ C$; Fig. 13	4.4	6.3	7.9	m Ω
		$V_{GS} = 10 V$; $I_D = 20 A$; $T_j = 105 ^\circ C$; Fig. 14	6.7	10	12.9	m Ω
		$V_{GS} = 10 V$; $I_D = 20 A$; $T_j = 125 ^\circ C$; Fig. 14	7.4	11	14.3	m Ω
		$V_{GS} = 10 V$; $I_D = 20 A$; $T_j = 175 ^\circ C$; Fig. 14	9.2	13.8	18.2	m Ω
		$V_{GS} = 4.5 V$; $I_D = 20 A$; $T_j = 25 ^\circ C$; Fig. 13	6.5	9.3	12.4	m Ω
		$V_{GS} = 4.5 V$; $I_D = 20 A$; $T_j = 105 ^\circ C$; Fig. 14	9.6	14.3	19.7	m Ω
		$V_{GS} = 4.5 V$; $I_D = 20 A$; $T_j = 125 ^\circ C$; Fig. 14	10.5	15.7	21.8	m Ω
		$V_{GS} = 4.5 V$; $I_D = 20 A$; $T_j = 175 ^\circ C$; Fig. 14	12.8	19.4	27.4	m Ω

Single N-channel 60 V, 7.9 mOhm logic level MOSFET in LPAK56 using Enhanced SOA technology

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		-	2.01	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 20 A; V _{DS} = 48 V; V _{GS} = 4.5 V; T _J = 25 °C; Fig. 15; Fig. 16		-	28	39.5	nC
		I _D = 20 A; V _{DS} = 48 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 15; Fig. 16		-	58	81	nC
Q _{GS}	gate-source charge	I _D = 20 A; V _{DS} = 48 V; V _{GS} = 4.5 V; T _J = 25 °C; Fig. 15; Fig. 16		-	8.2	12.3	nC
Q _{GD}	gate-drain charge			-	11.7	23.3	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 17		-	3229	4520	pF
C _{oss}	output capacitance			-	301	361	pF
C _{rss}	reverse transfer capacitance			-	156	213	pF
t _{d(on)}	turn-on delay time	V _{DS} = 48 V; R _L = 2.4 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	16	-	ns
t _r	rise time			-	39	-	ns
t _{d(off)}	turn-off delay time			-	34	-	ns
t _f	fall time			-	29	-	ns
g _{fs}	transfer conductance	V _{DS} = 8 V; I _D = 20 A; T _J = 25 °C; Fig. 9		-	62.5	-	S
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 20 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 18		-	0.82	1	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 30 V; T _J = 25 °C; Fig. 19		-	28	-	ns
Q _r	recovered charge		[1]	-	30	-	nC

[1] includes capacitive recovery

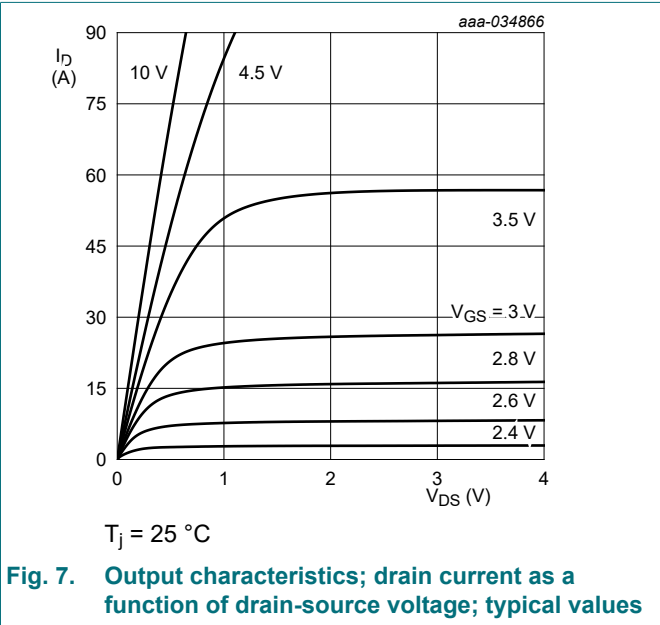


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

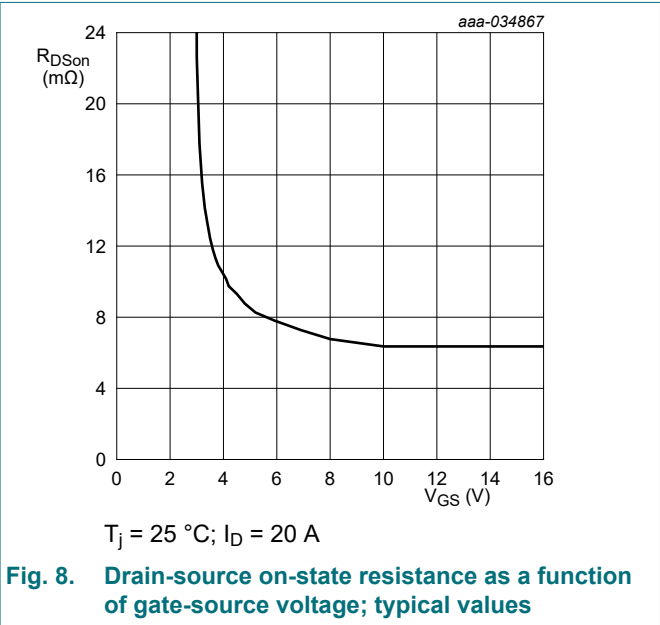


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

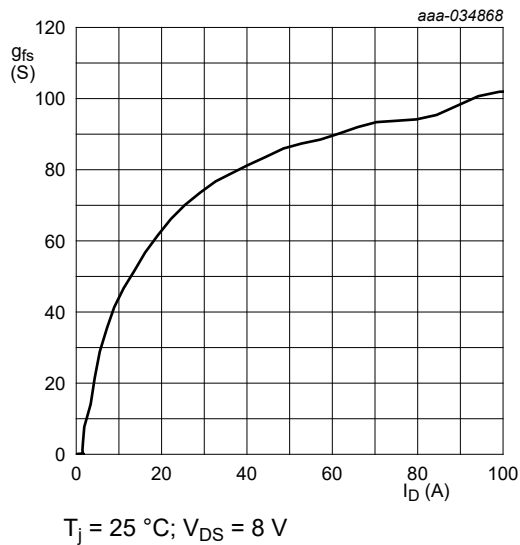


Fig. 9. Forward transconductance as a function of drain current; typical values

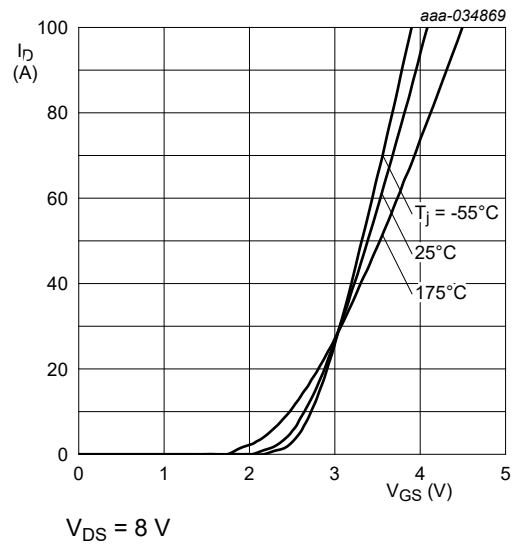


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

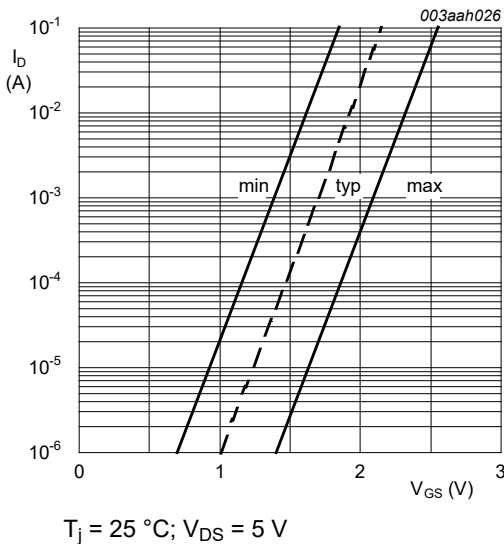


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

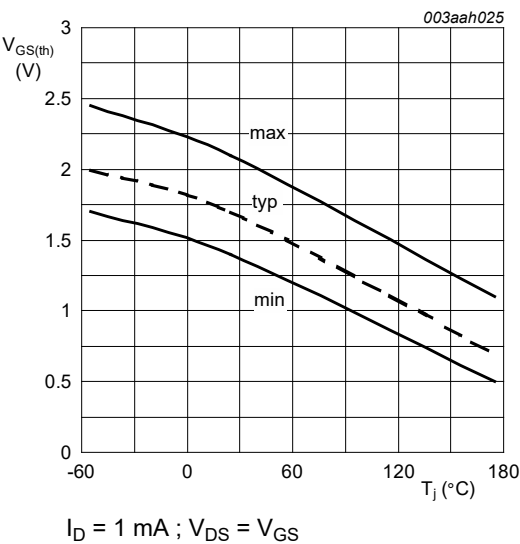


Fig. 12. Gate-source threshold voltage as a function of junction temperature

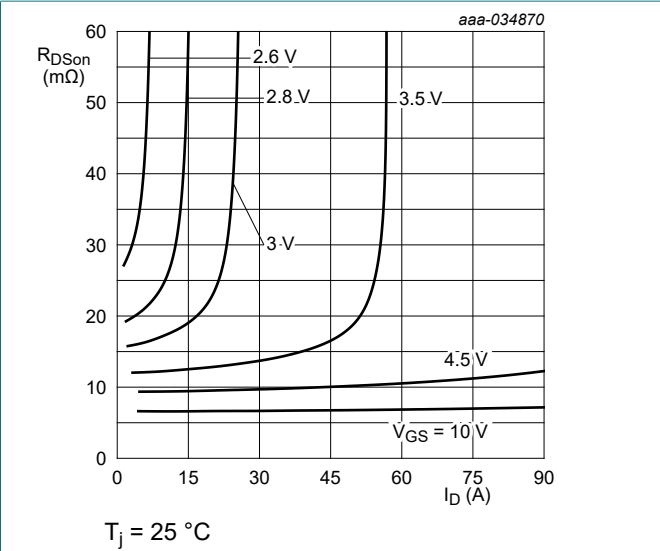


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

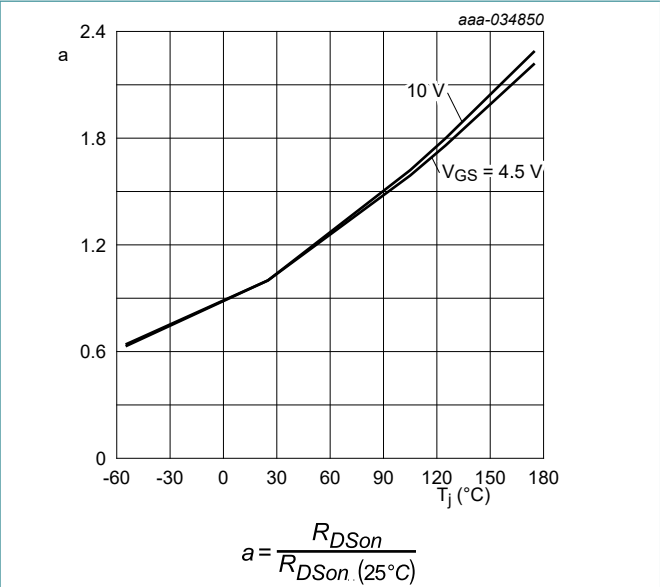


Fig. 14. Normalized drain-source on-state resistance factor as a function of junction temperature

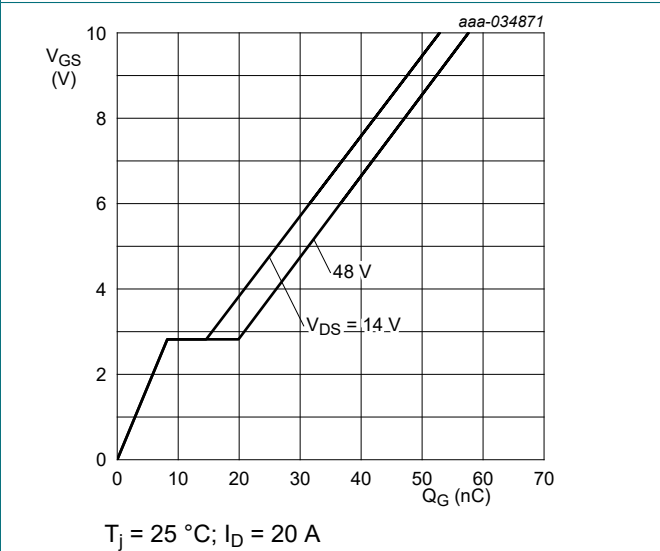


Fig. 15. Gate-source voltage as a function of gate charge; typical values

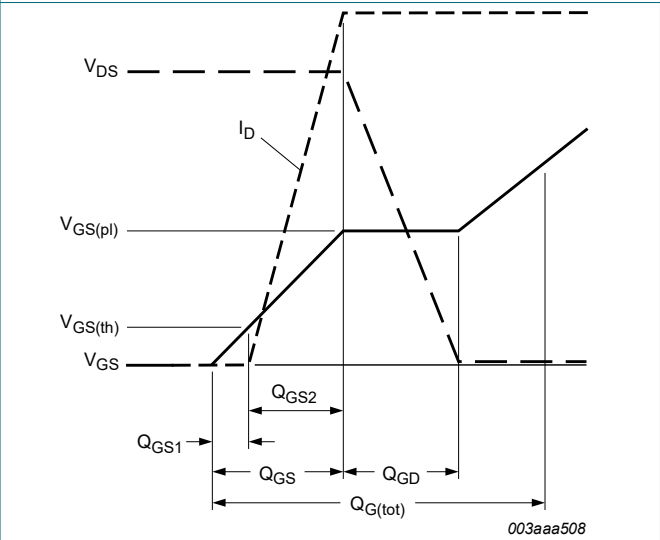


Fig. 16. Gate charge waveform definitions

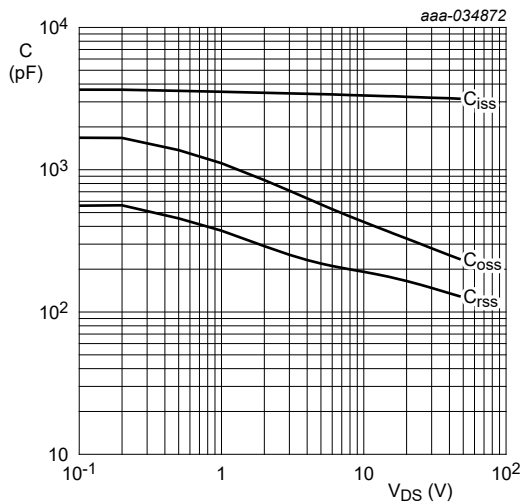


Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

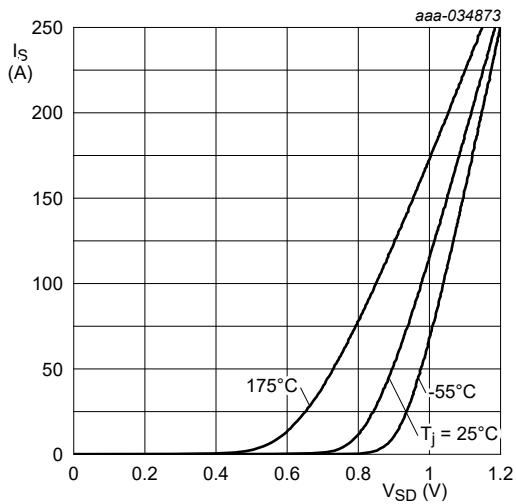


Fig. 18. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

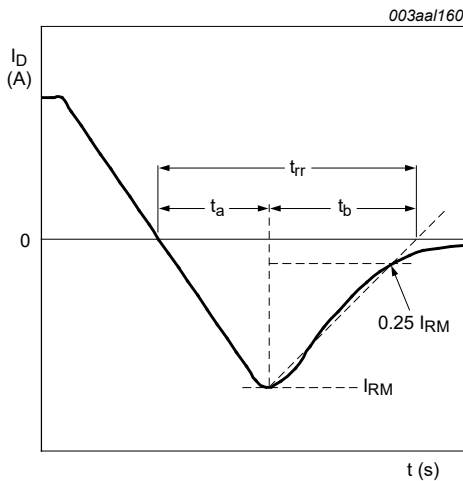


Fig. 19. Reverse recovery timing definition

11. Package outline

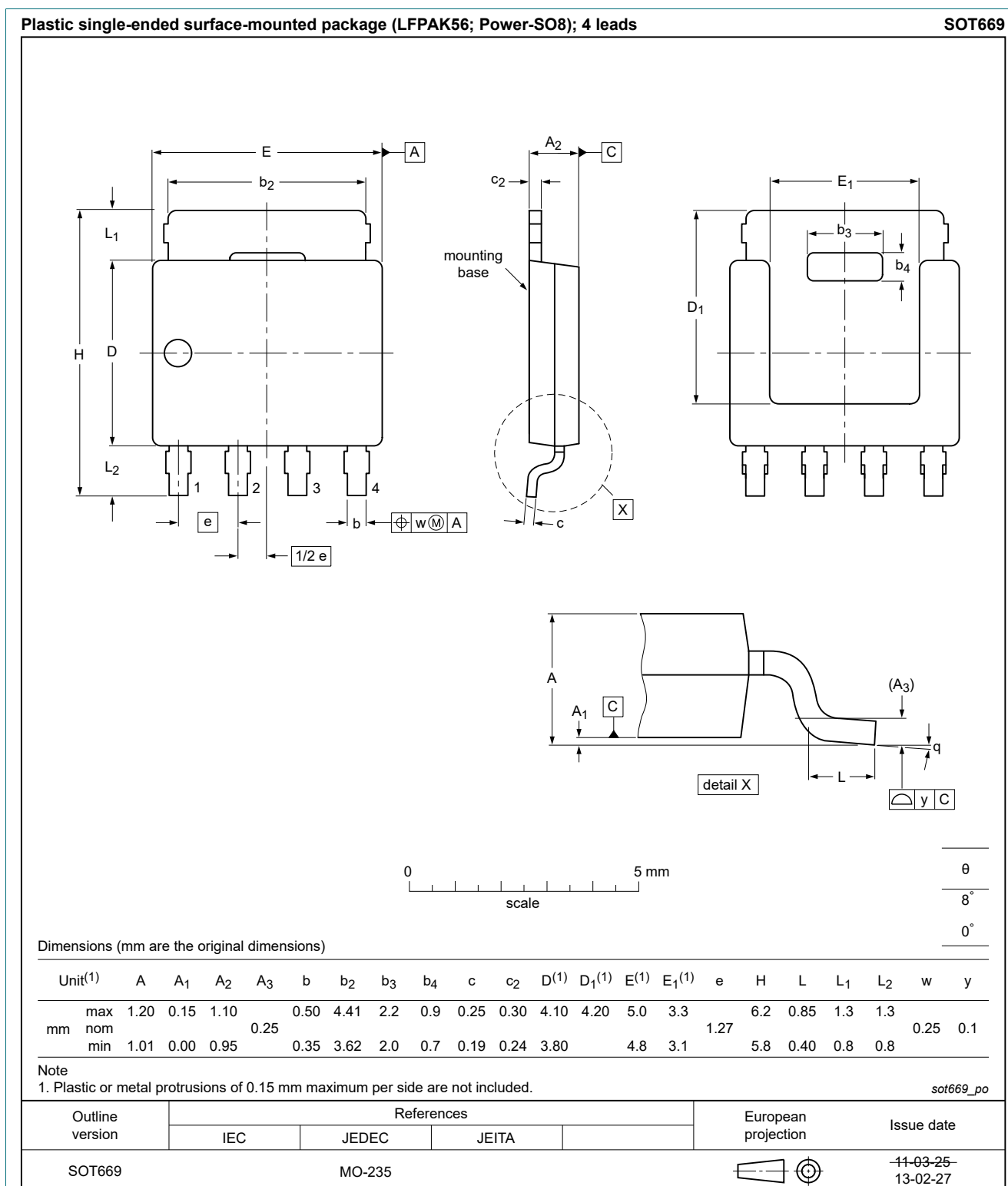


Fig. 20. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	2
9. Thermal characteristics.....	4
10. Characteristics.....	5
11. Package outline.....	10
12. Legal information.....	11

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