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MOSFET - Power, Single N-Channel

100 V, 26 mΩ, 28 A

NVTF5027N10MCL

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTF5027N10MCL – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	100	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Note 1)	Steady State	T _C = 25°C	I _D	28	A
		T _C = 100°C		20	
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	P _D	46	W
		T _C = 100°C		23	
Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	I _D	7.4	A
		T _A = 100°C		5.2	
Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25°C	P _D	3.1	W
		T _A = 100°C		1.6	
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	119	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	–55 to +175	°C
Source Current (Body Diode)			I _S	35	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 1.3 A)			E _{AS}	414	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	3.3	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	47.7	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.

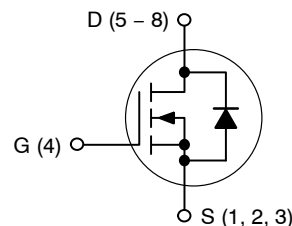


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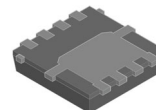
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$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	26 mΩ @ 10 V	28 A
	35 mΩ @ 4.5 V	

N-Channel

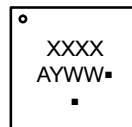
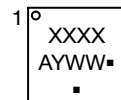


WDFN8
(μ8FL)
CASE 511AB



WDFNW8
(μ8FL WF)
CASE 515AN

MARKING DIAGRAMS



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVTF5027N10MCL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			53		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V	T _J = 25°C		1.0	μA
			T _J = 125°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 38 μA	1		3	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-6		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7 A		21	26	mΩ
		V _{GS} = 4.5 V, I _D = 5 A		28	35	
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 7 A		25		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 50 V		800		pF
Output Capacitance	C _{OSS}			300		
Reverse Transfer Capacitance	C _{RSS}			4		
Gate Resistance	R _G			0.41		Ω
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 50 V; I _D = 7 A		5.5		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 7 A		11.5		
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 7 A		1.3		nC
Gate-to-Source Charge	Q _{GS}			2.1		
Gate-to-Drain Charge	Q _{GD}			1.2		
Plateau Voltage	V _{GP}			2.5		V

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 50 V, I _D = 7 A		7.4		ns
Rise Time	t _r			2		
Turn-Off Delay Time	t _{d(OFF)}			19		
Fall Time	t _f			2.9		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 7 A, T _J = 25°C		0.84	1.3	V
		V _{GS} = 0 V, I _S = 7 A, T _J = 125°C		0.73		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 3 A		28		ns
Reverse Recovery Charge	Q _{RR}			17		nC
Charge Time	t _a			13.9		ns
Discharge Time	t _b			14.2		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

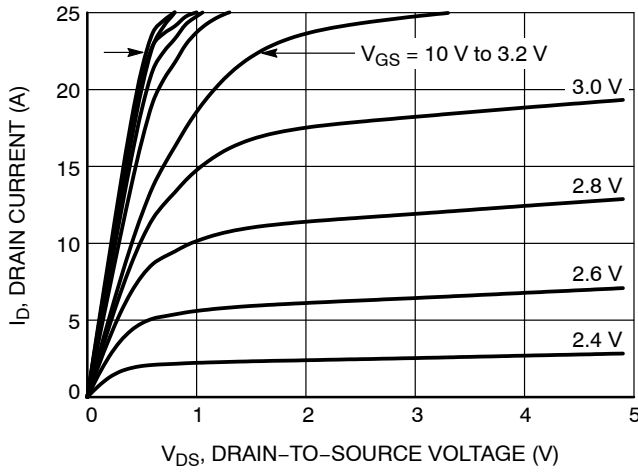


Figure 1. On-Region Characteristics

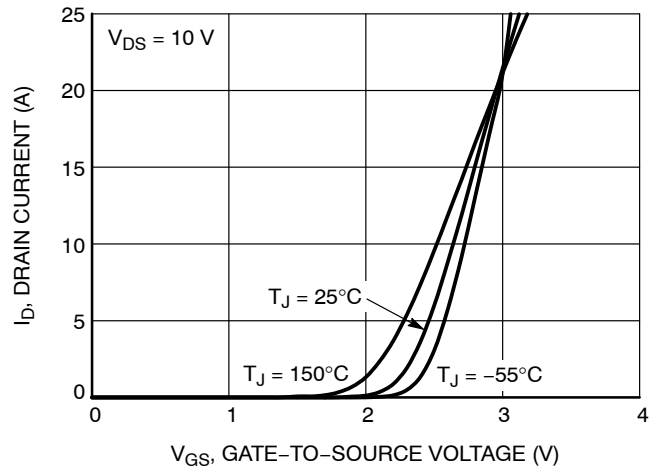


Figure 2. Transfer Characteristics

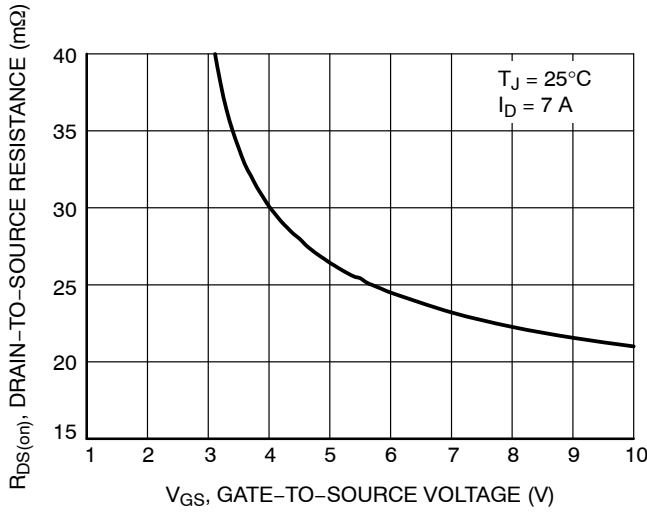


Figure 3. On-Resistance vs. Gate-to-Source Voltage

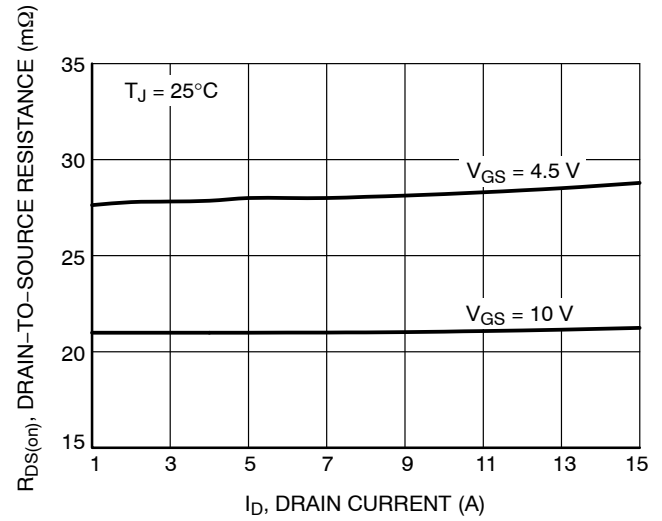


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

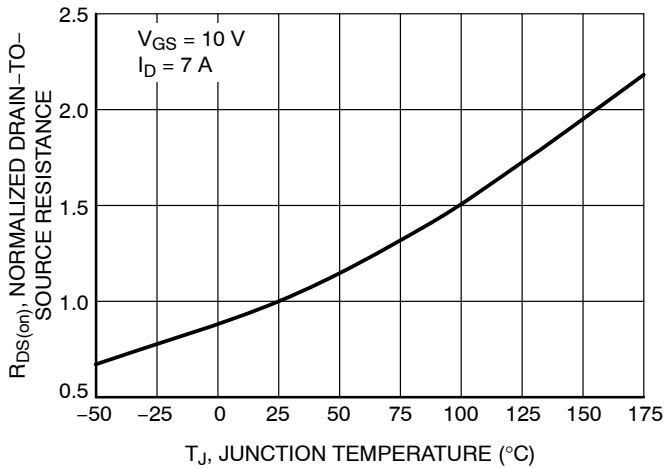


Figure 5. On-Resistance Variation with Temperature

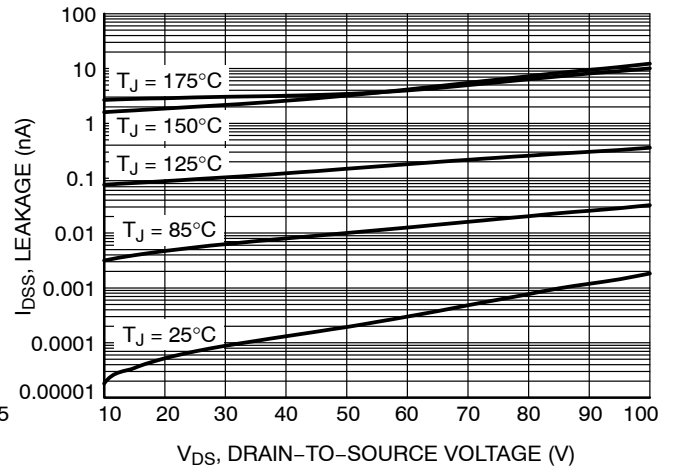


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

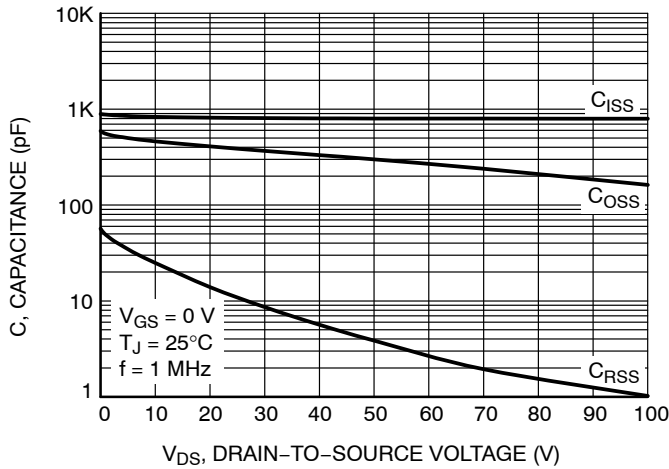


Figure 7. Capacitance Variation

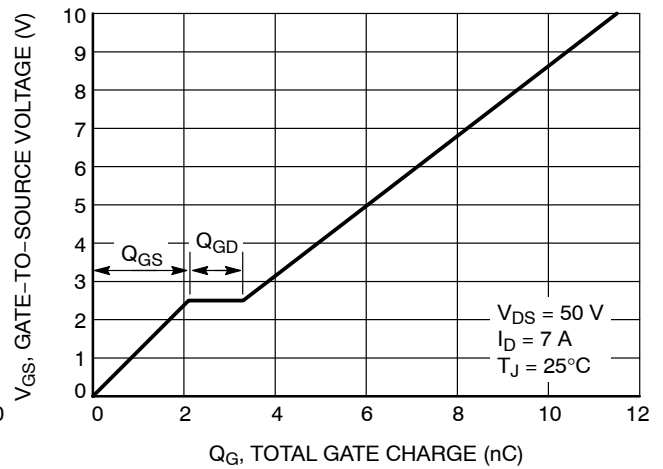


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

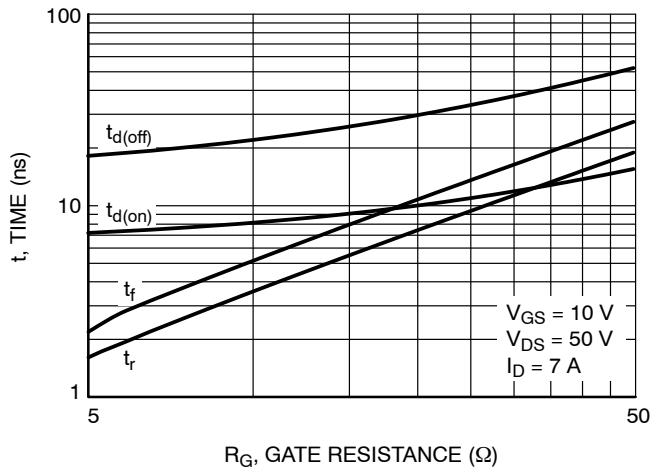


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

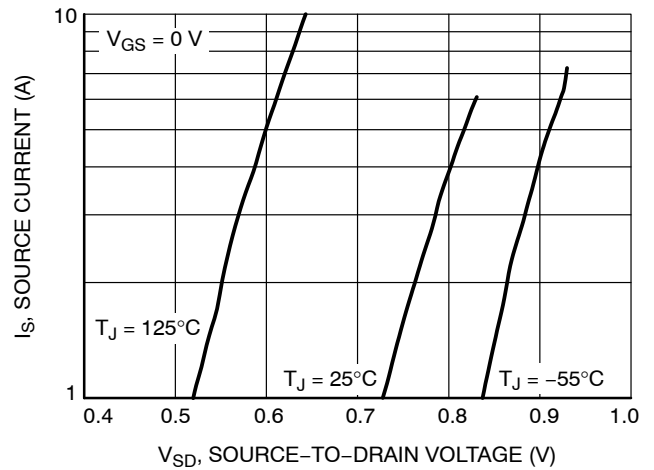


Figure 10. Diode Forward Voltage vs. Current

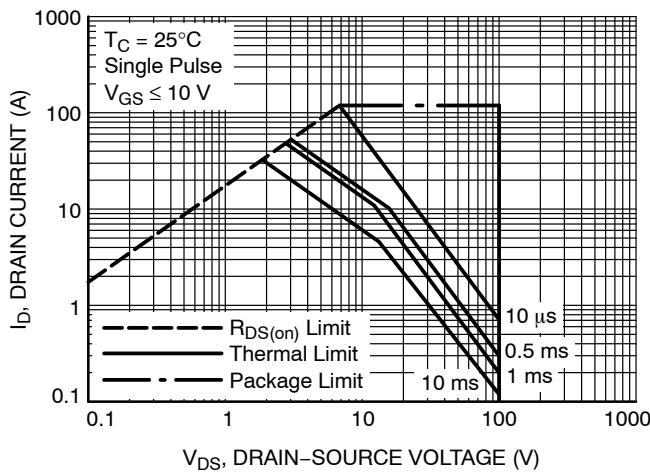


Figure 11. Safe Operating Area

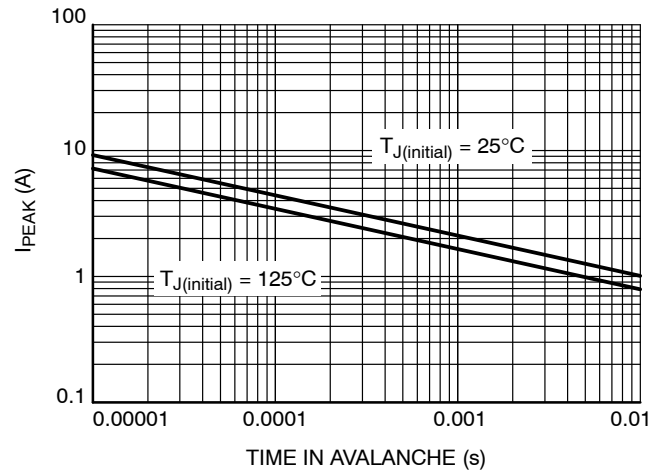


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVTFS027N10MCL

TYPICAL CHARACTERISTICS

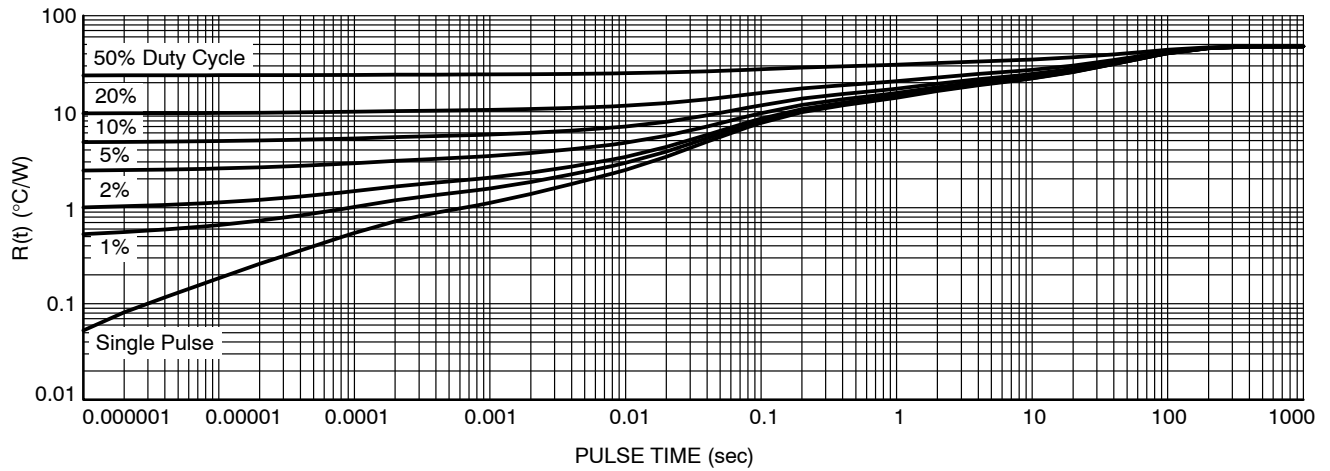


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

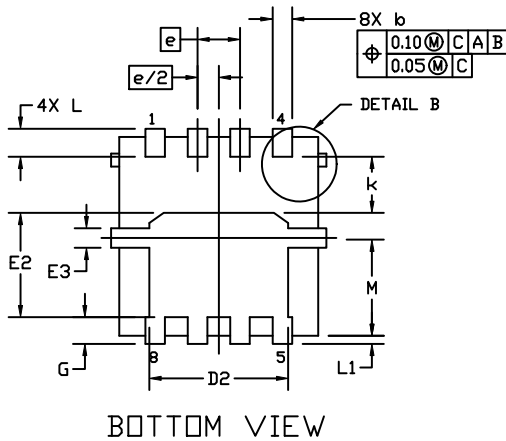
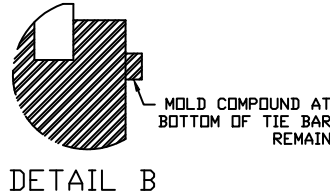
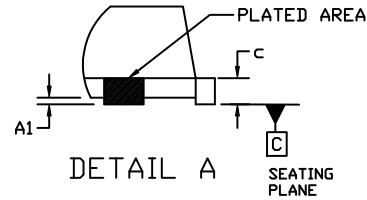
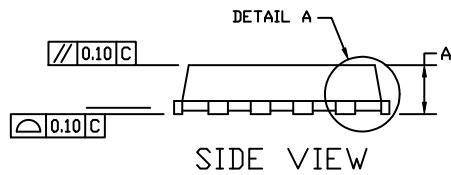
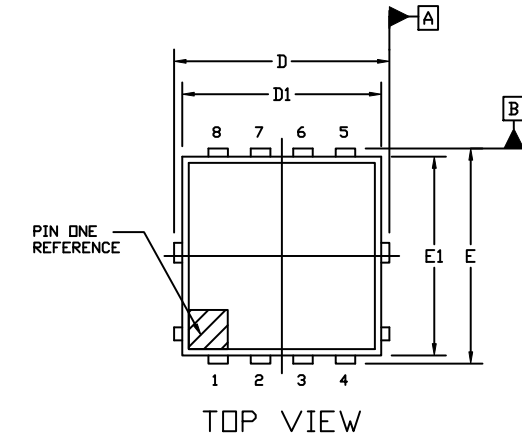
Device	Marking	Package	Shipping [†]
NVTFS027N10MCLTAG	27L1	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFWS027N10MCLTAG	27W1	WDFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVTFS027N10MCL

PACKAGE DIMENSIONS

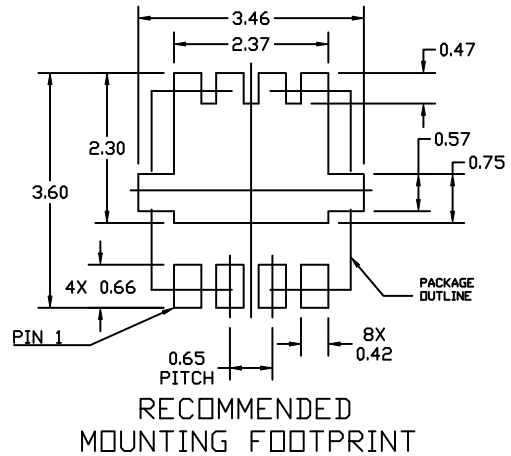
WDFNW8 3.3x3.3, 0.65P (Full-Cut μ 8FL WF) CASE 515AN ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

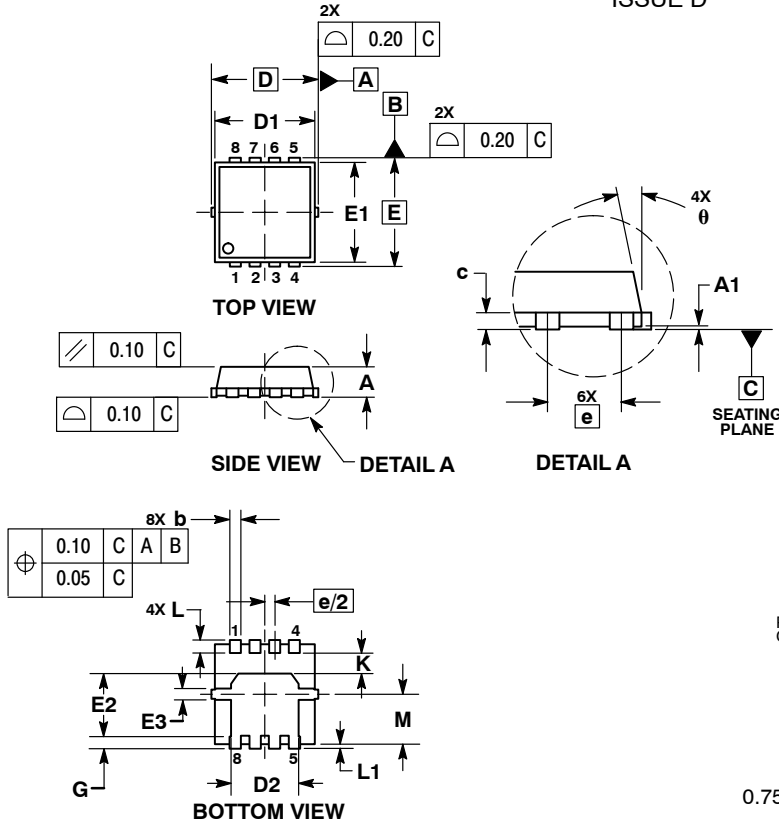
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

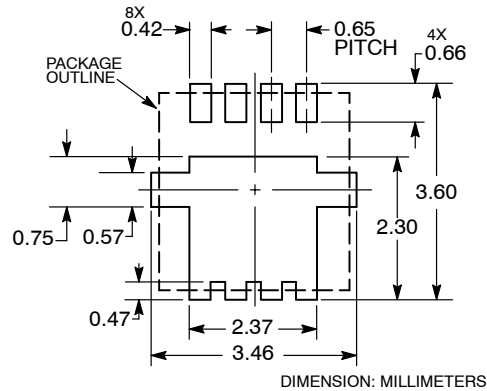
WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °			0 °		

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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