



PXP020-20QX

20 V, P-channel Trench MOSFET

26 October 2021

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Trench MOSFET technology
- MLPAK33 package (3.3 x 3.3 mm footprint)

3. Applications

- High-side load switch
- Battery management
- DC-to-DC conversion
- Switching circuits

4. Quick reference data

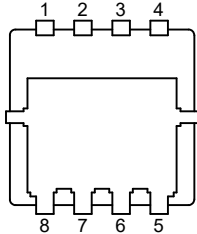
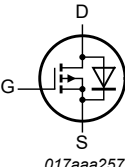
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	-20	V
V_{GS}	gate-source voltage			-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-	-12.1	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -7.7\text{ A}; T_j = 25\text{ °C}$		-	16	20	mΩ
		$V_{GS} = -2.5\text{ V}; I_D = -5.8\text{ A}; T_j = 25\text{ °C}$		-	26.4	35.2	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	 017aaa257
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXP020-20QX	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXP020-20QX	8AD

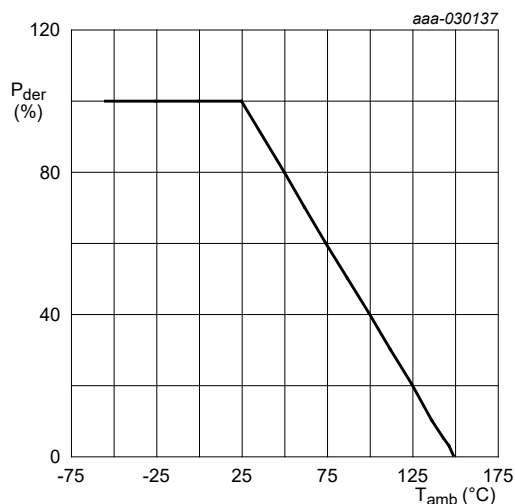
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

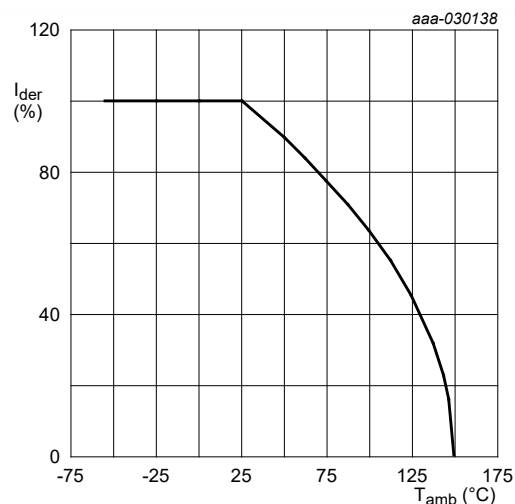
Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-12.1	A
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-8	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-4.8	A
		V _{GS} = -4.5 V; T _{sp} = 25 °C		-	-23.5	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-42.4	A
P _{tot}	total power dissipation	T _{amb} = 25 °C; t ≤ 5 s	[1]	-	4.2	W
		T _{amb} = 25 °C	[1]	-	1.7	W
		T _{sp} = 25 °C		-	15	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.7	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



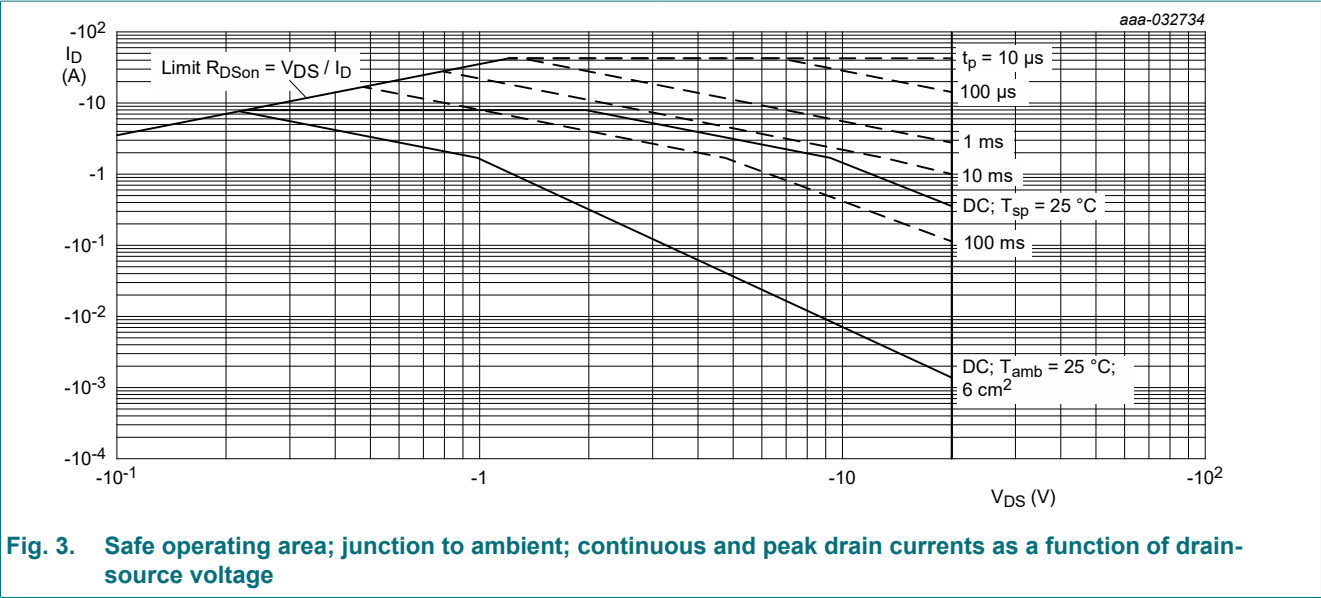
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}\text{C})} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_D(25^{\circ}\text{C})} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of ambient temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	150	190	K/W
			[2]	-	60	75	K/W
		in free air; $t \leq 5$ s	[2]	-	25	30	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	4	8	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

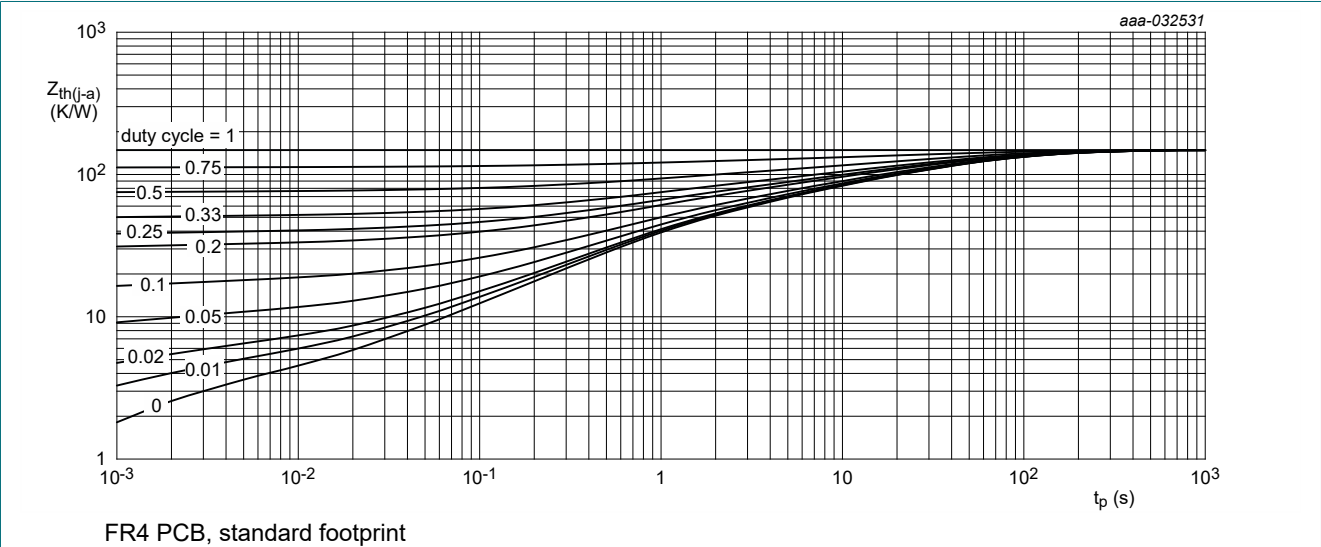


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

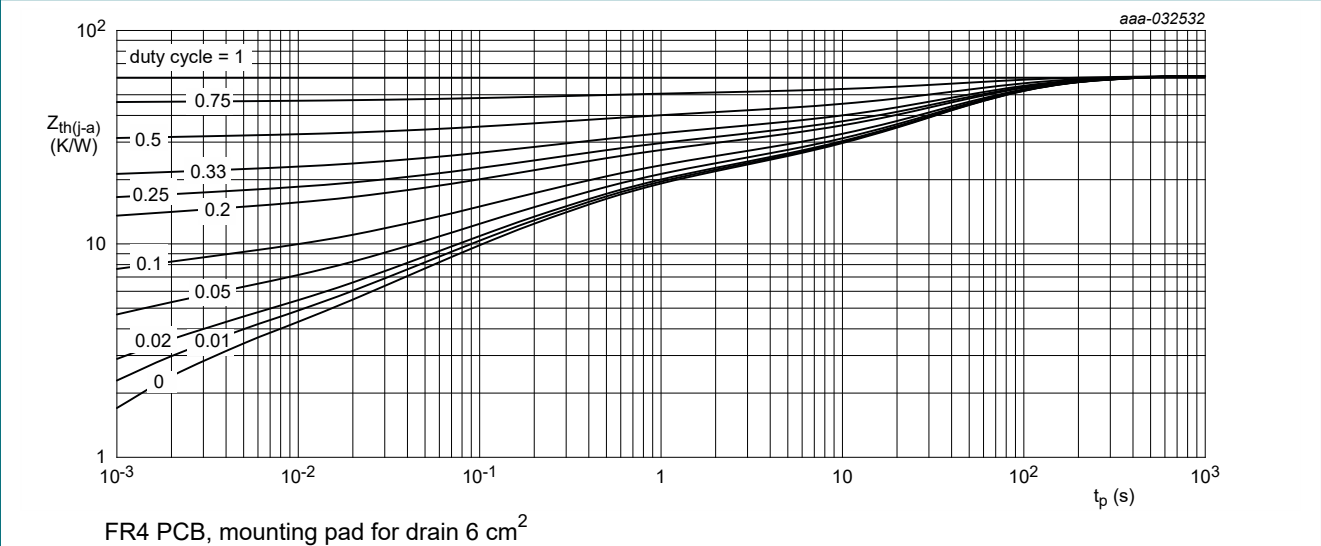


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		-0.7	-0.9	-1.25	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -7.7 A; T _j = 25 °C		-	16	20	mΩ
		V _{GS} = -4.5 V; I _D = -7.7 A; T _j = 150 °C		-	22.7	28.4	mΩ
		V _{GS} = -2.5 V; I _D = -5.8 A; T _j = 25 °C		-	26.4	35.2	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -7.7 A; T _j = 25 °C		-	21.4	-	S
R _G	gate resistance	f = 1 MHz		-	6.4	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -7.7 A; V _{GS} = -4.5 V; T _j = 25 °C		-	19.4	29.1	nC
Q _{GS}	gate-source charge			-	3.4	-	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	1.6	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	1.8	-	nC
Q _{GD}	gate-drain charge			-	6.2	-	nC
V _{GSpl}	gate-source plateau voltage	V _{DS} = -10 V; I _D = -7.7 A; T _j = 25 °C		-	-1.8	-	V
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	1900	-	pF
C _{oss}	output capacitance			-	275	-	pF
C _{rss}	reverse transfer capacitance			-	250	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -5.8 A; V _{GS} = -4.5 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	6	-	ns
t _r	rise time			-	23	-	ns
t _{d(off)}	turn-off delay time			-	46	-	ns
t _f	fall time			-	31	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -1.7 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V
t _{rr}	reverse recovery time	I _S = -1.7 A; dI _S /dt = 100 A/μs; V _{GS} = -4.5 V; V _{DS} = -10 V; T _j = 25 °C		-	26	-	ns
Q _r	recovered charge			-	10	-	nC
t _a	reverse recovery rise time			-	6	-	ns
t _b	reverse recovery fall time			-	20	-	ns

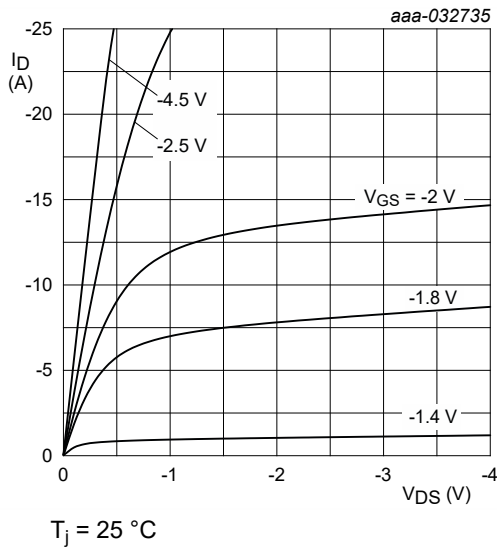


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

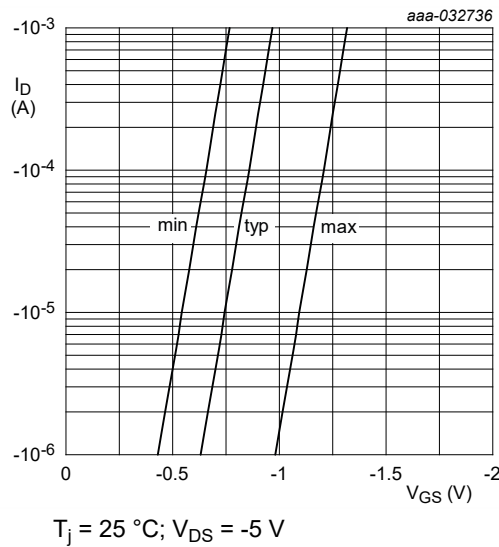


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

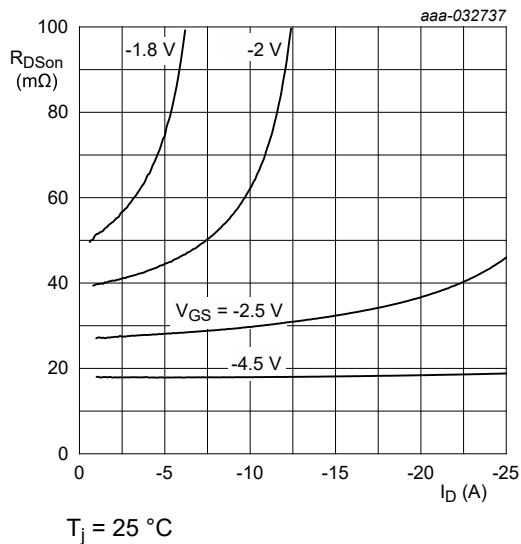


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

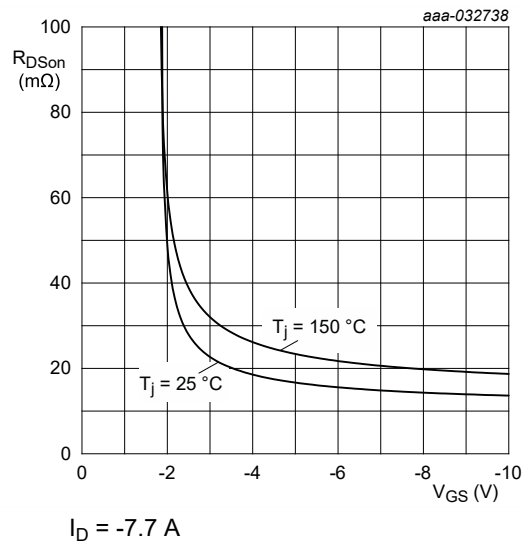


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

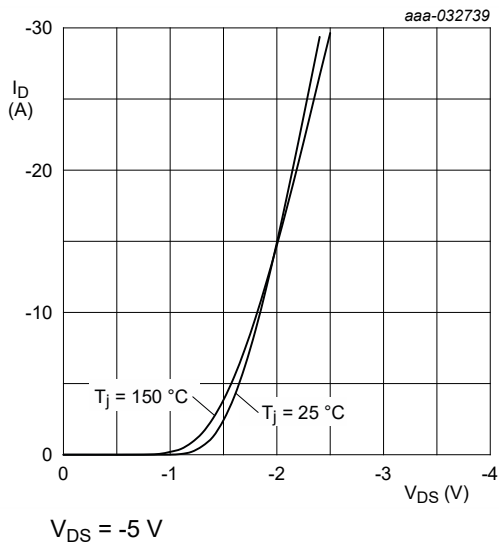


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

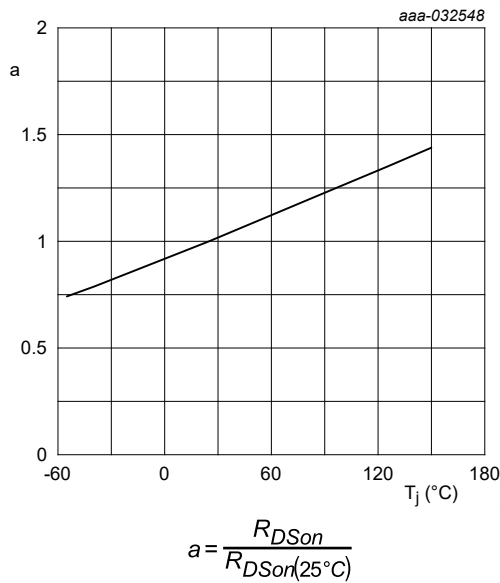


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

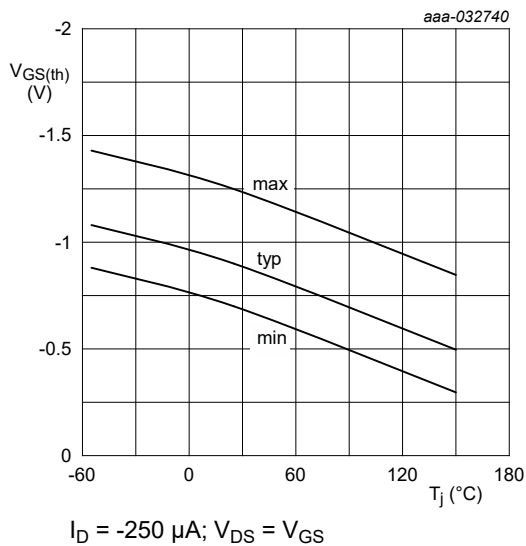


Fig. 12. Gate-source threshold voltage as a function of junction temperature

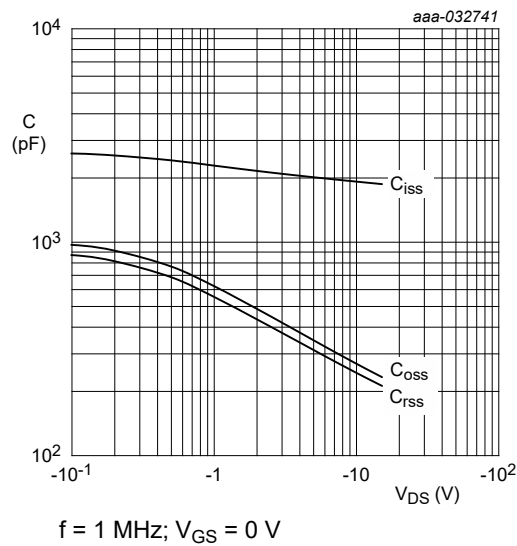


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

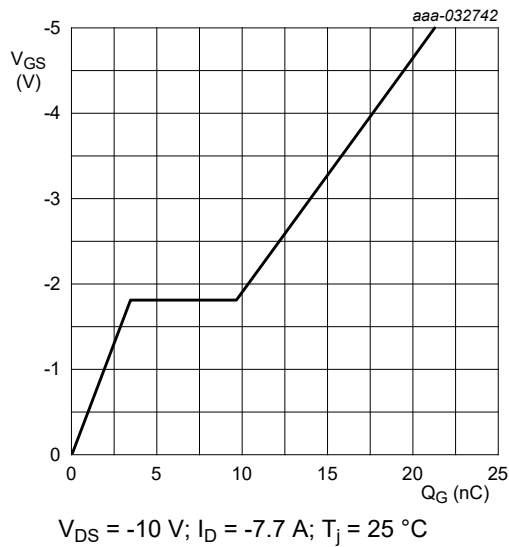


Fig. 14. Gate-source voltage as a function of gate charge; typical values

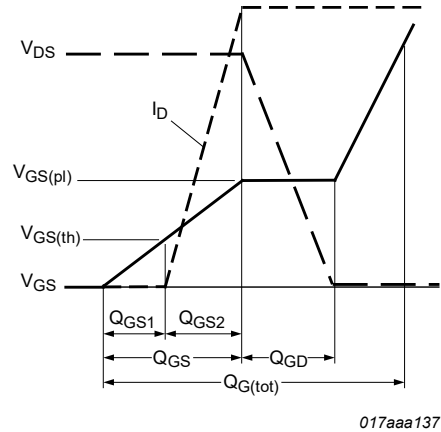


Fig. 15. Gate charge waveform definitions

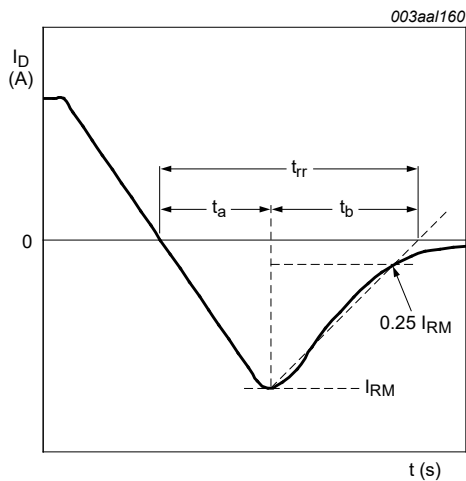


Fig. 16. Reverse recovery timing definition

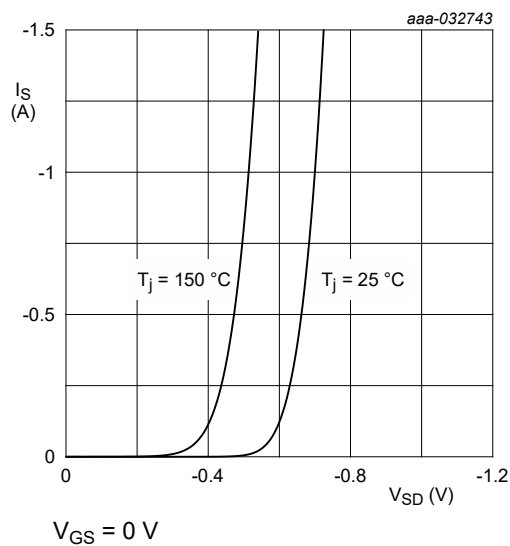


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

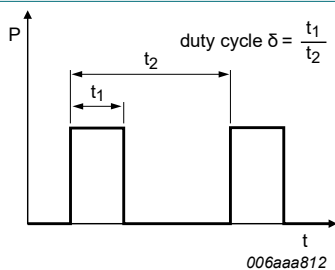
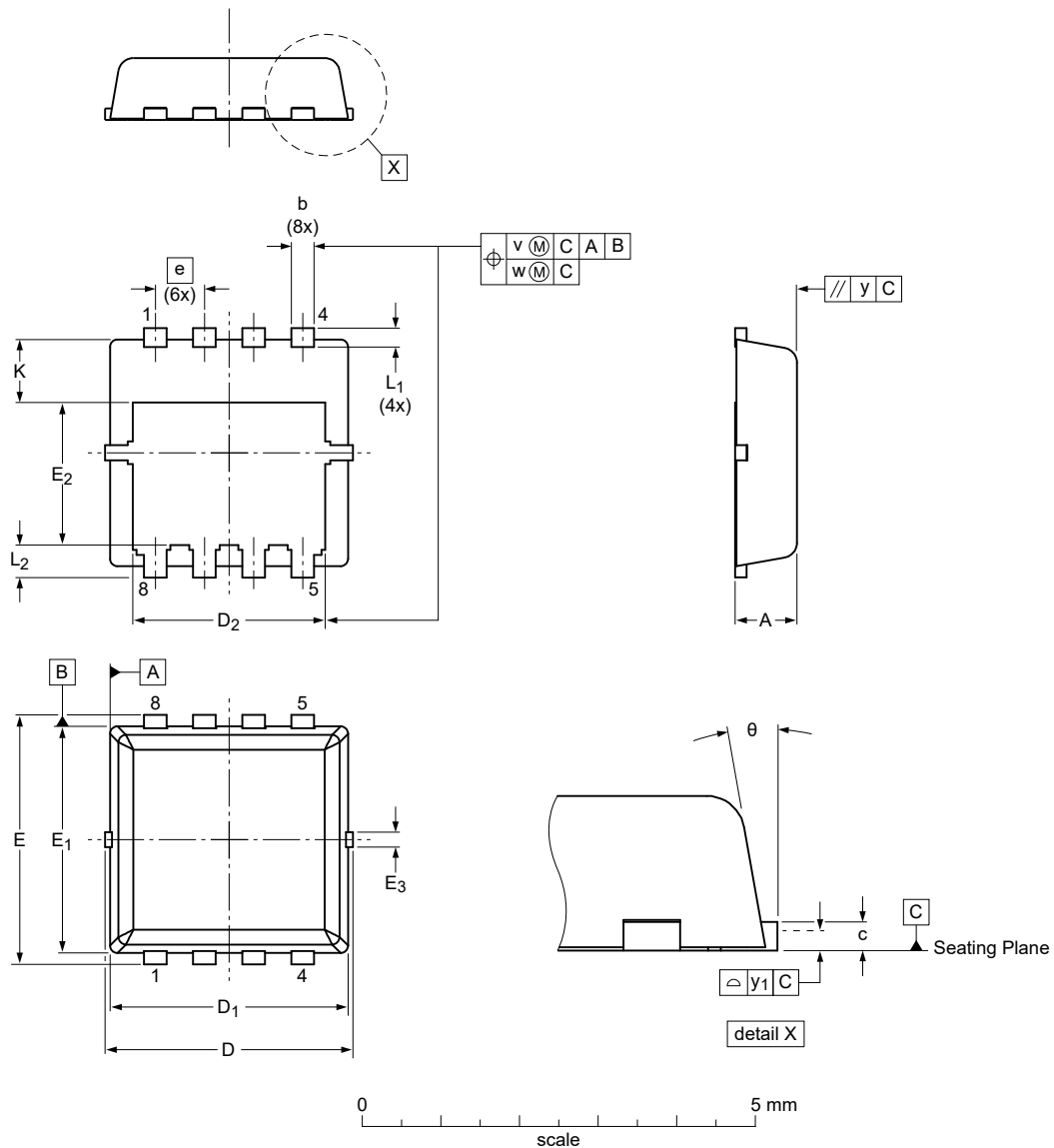


Fig. 18. Duty cycle definition

12. Package outline

MLPAK33: plastic thermal enhanced surface mounted package; mini leads; 8 terminals;
pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body

SOT8002-1



Dimensions (mm are the original dimensions)

Unit	A	b	c	D	D ₁	D ₂	e	E	E ₁	E ₂	E ₃	K	L ₁	L ₂	θ	y	y ₁	v	w
max	0.90	0.35	0.18	3.50	3.25	2.65		3.50	3.10	1.99	0.25		0.40	0.58	12°				
nom	0.80	0.30	0.15	3.30	3.15	2.55	0.65	3.30	3.00	1.89	0.20	0.65 (ref)	0.25	0.43	10°	0.05	0.05	0.1	0.05
min	0.70	0.25	0.12	3.10	3.05	2.45		3.10	2.90	1.79	0.15		0.10	0.28	8°				

sot8002-1_po

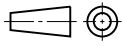
Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT8002-1						19-12-19 20-01-09

Fig. 19. Package outline MLPAK33 (SOT8002-1)

13. Soldering

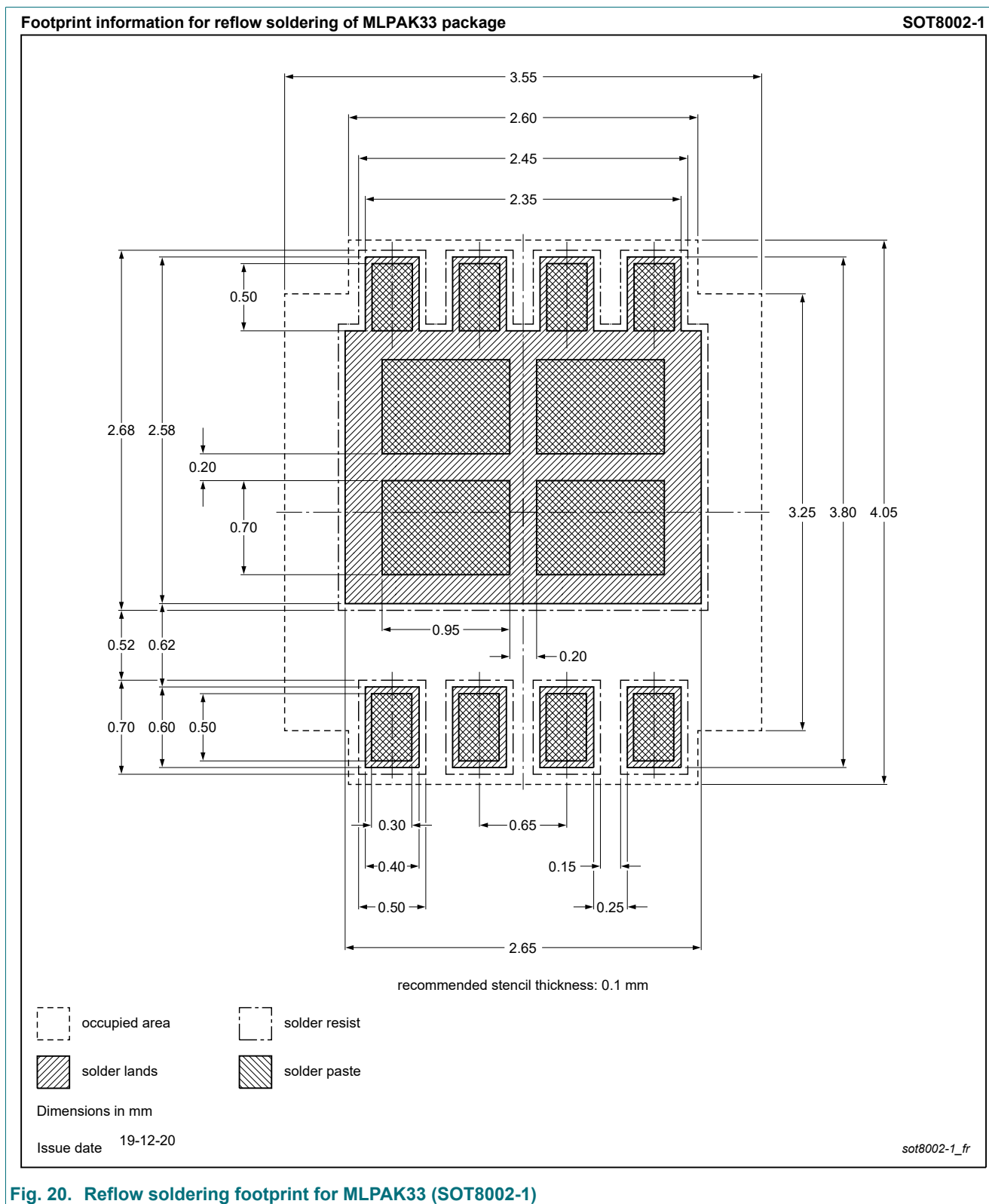


Fig. 20. Reflow soldering footprint for MLPAK33 (SOT8002-1)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PXP020-20QX v.2	20211026	Product data sheet	-	PXP020-20QX v.1
Modifications:	Chapter "Limiting values": P_{tot} corrected, now matching the data in chapter "Thermal characteristics"			
PXP020-20QX v.1	20210414	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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