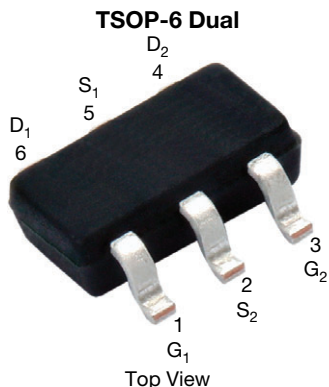


Automotive Dual P-Channel 30 V (D-S) 175 °C MOSFET



Marking Code: 9B

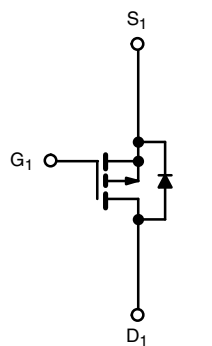
PRODUCT SUMMARY	
V_{DS} (V)	-30
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	-0.155
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	-0.300
I_D (A)	-2.32
Configuration	Dual
Package	TSOP-6

FEATURES

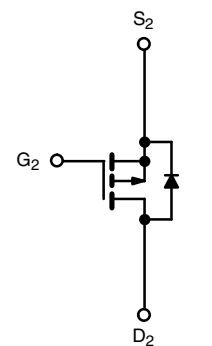
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-30	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C) ^a	$T_C = 25$ °C	I_D	-2.5	A
	$T_C = 125$ °C		-1.5	
Pulsed drain current		I_{DM}	-10.2	
Continuous source current (diode conduction) ^a		I_S	-2.1	
Maximum power dissipation ^a	$T_C = 25$ °C	P_D	1.67	W
	$T_C = 125$ °C		0.56	
Unclamped inductive surge UIS		I_{AV}	7	A
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Maximum junction-to-ambient ^a	Steady state	R_{thJA}	150	°C/W
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	90	

Note

a. Surface mounted on 1" x 1" FR4 board



SPECIFICATIONS (T _J = 25°C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-0.6	-	-1.5	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = -30 V	-	-	-1	μA
		V _{GS} = 0 V	V _{DS} = -30 V, T _J = 55 °C	-	-	-5	
On-state drain current ^a	I _{D(on)}	V _{GS} = -10 V	V _{DS} ≤ -5 V	-4	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V	I _D = -0.4 A	-	0.140	0.155	Ω
		V _{GS} = -4.5 V	I _D = -0.2 A	-	0.265	0.300	
Forward transconductance ^a	g _{fs}	V _{DS} = -5 V, I _D = -1 A		-	2.2	-	S
Diode forward voltage ^a	V _{SD}	I _S = -0.5 A, V _{GS} = 0 V		-	-0.83	-1.1	V
Dynamic ^b							
Total gate charge	Q _g	V _{GS} = -10 V	V _{DS} = -15 V, I _D = -3 A	-	8.6	11.1	nC
Gate-source charge	Q _{gs}			-	1.2	-	
Gate-drain charge	Q _{gd}			-	3	-	
Gate resistance	R _g	f = 1 MHz		2.5	-	7.2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 1 kΩ		-	5.7	8	ns
Rise time	t _r			-	3	4	
Turn-off delay time	t _{d(off)}			-	13.8	18	
Fall time	t _f			-	2	3	

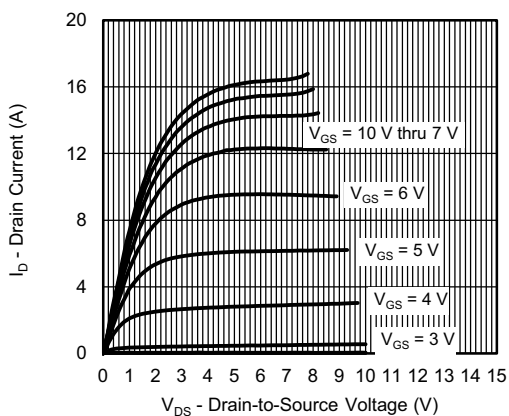
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$
b. Guaranteed by design, not subject to production testing

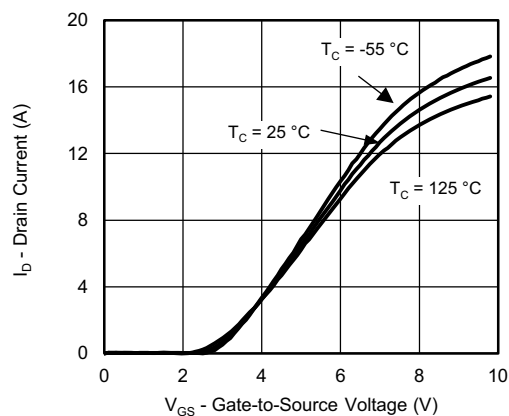
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



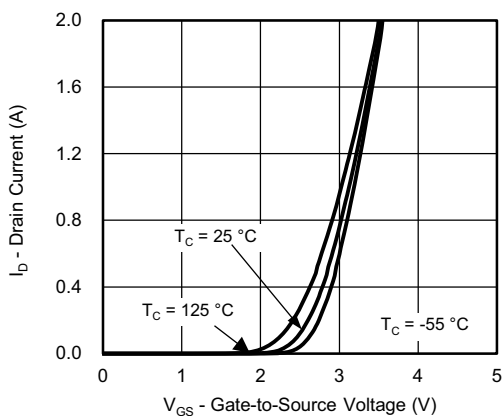
TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



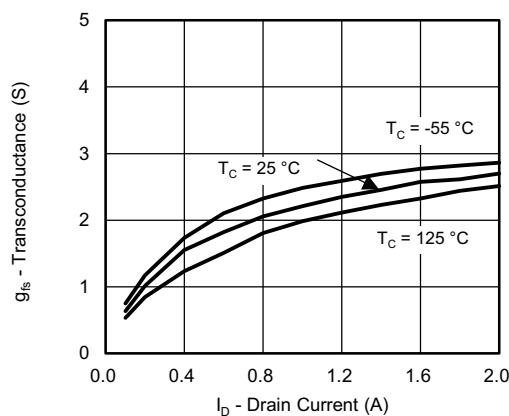
Output Characteristics



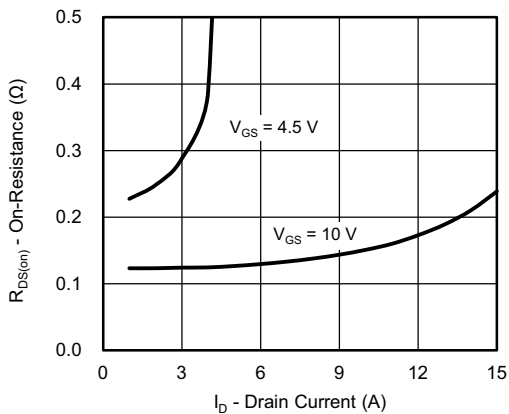
Transfer Characteristics



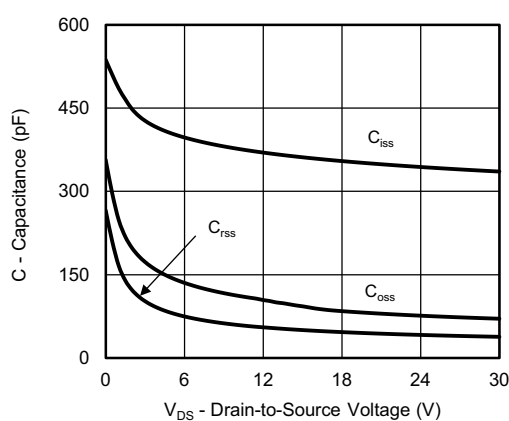
Transfer Characteristics



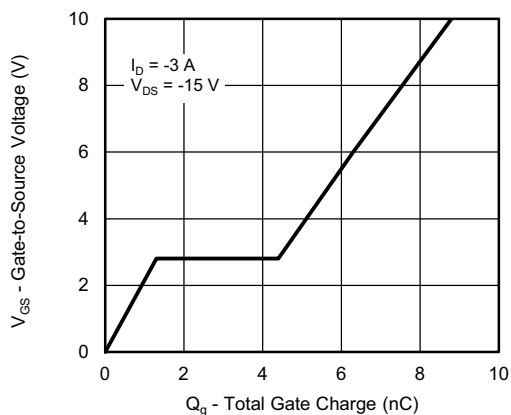
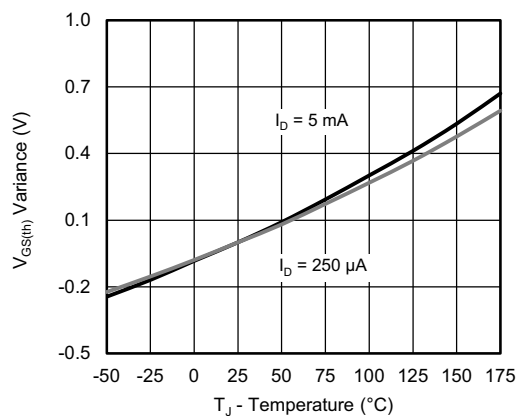
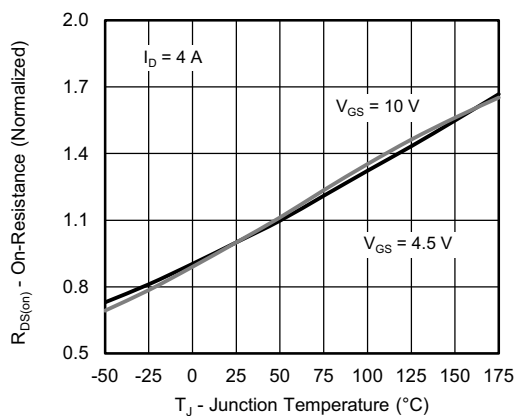
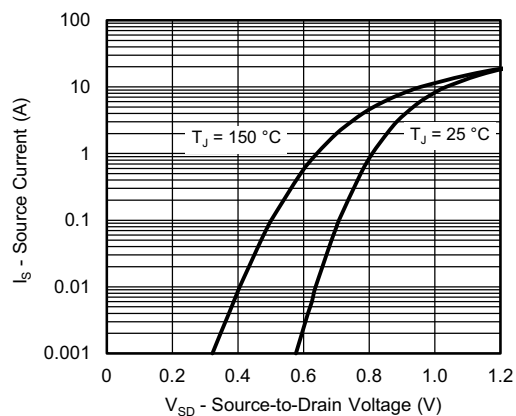
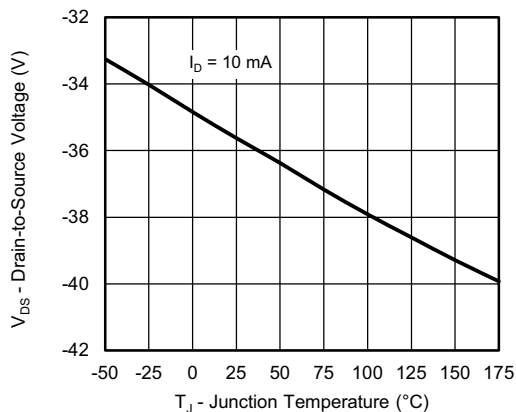
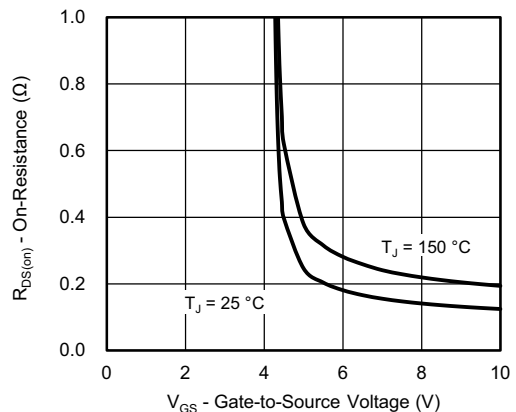
Transconductance

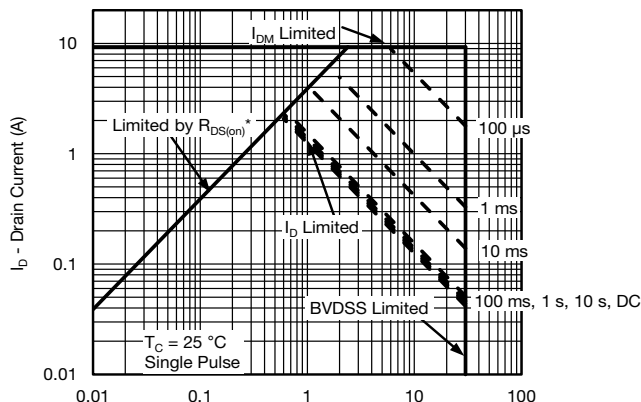


On-Resistance vs. Drain Current

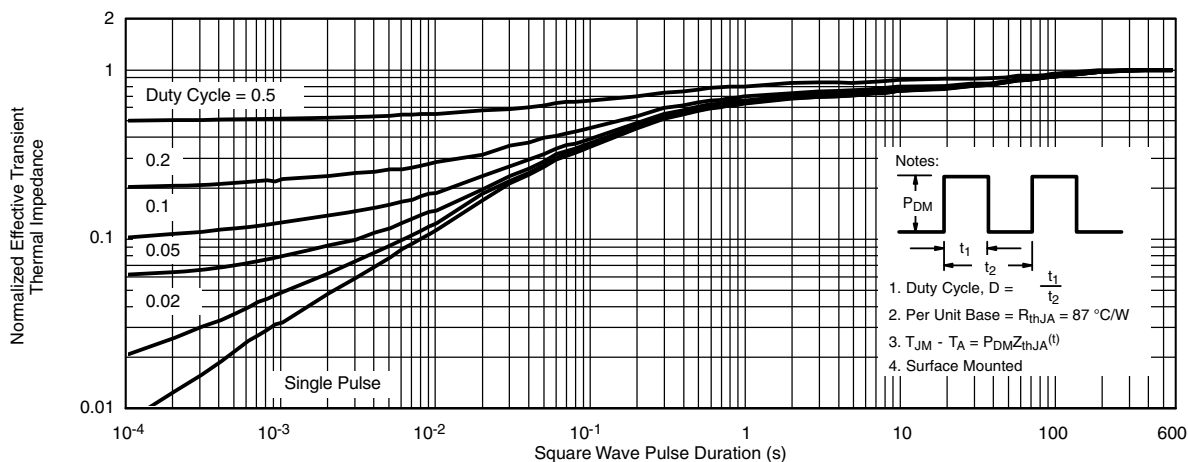
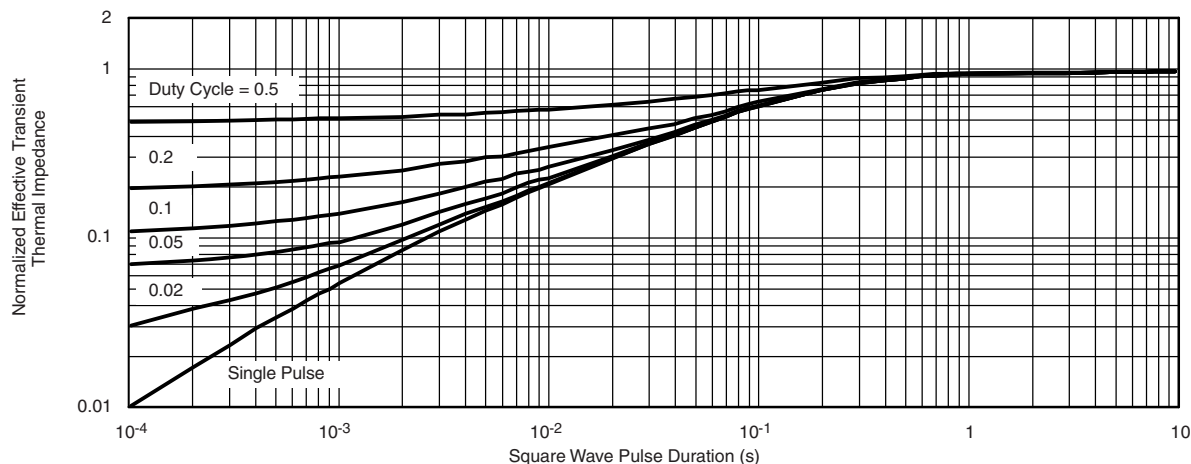


Capacitance

TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

Gate Charge

Threshold Voltage

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

Drain Source Breakdown vs. Junction Temperature

On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

 V_{DS} - Drain-to-Source Voltage (V)

 $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

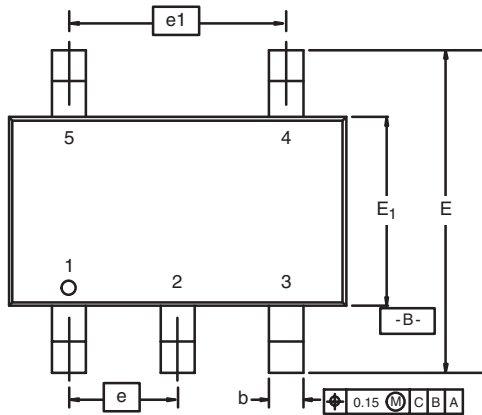
Safe Operating Area, Junction-to-Case

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75059.

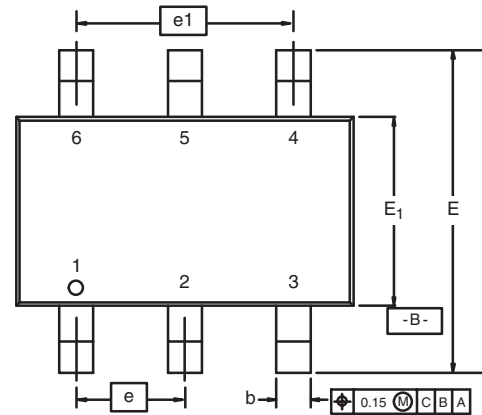


TSOP: 5/6-LEAD

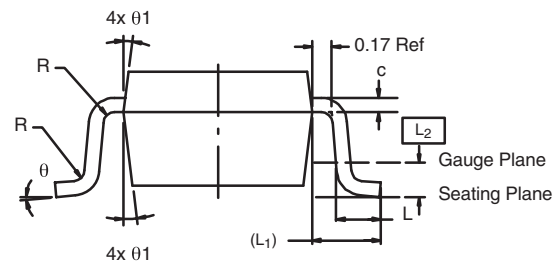
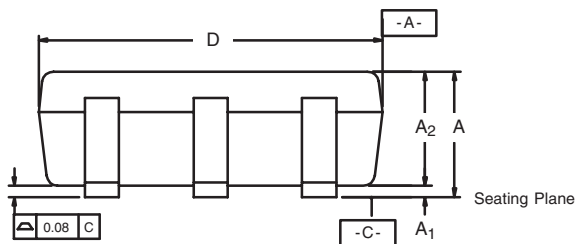
JEDEC Part Number: MO-193C



5-LEAD TSOP

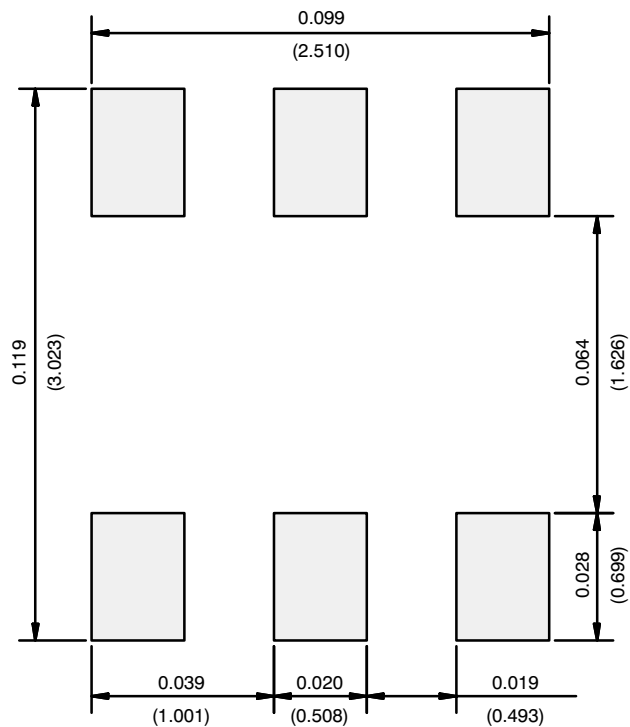


6-LEAD TSOP



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads
Dimensions in Inches/(mm)

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