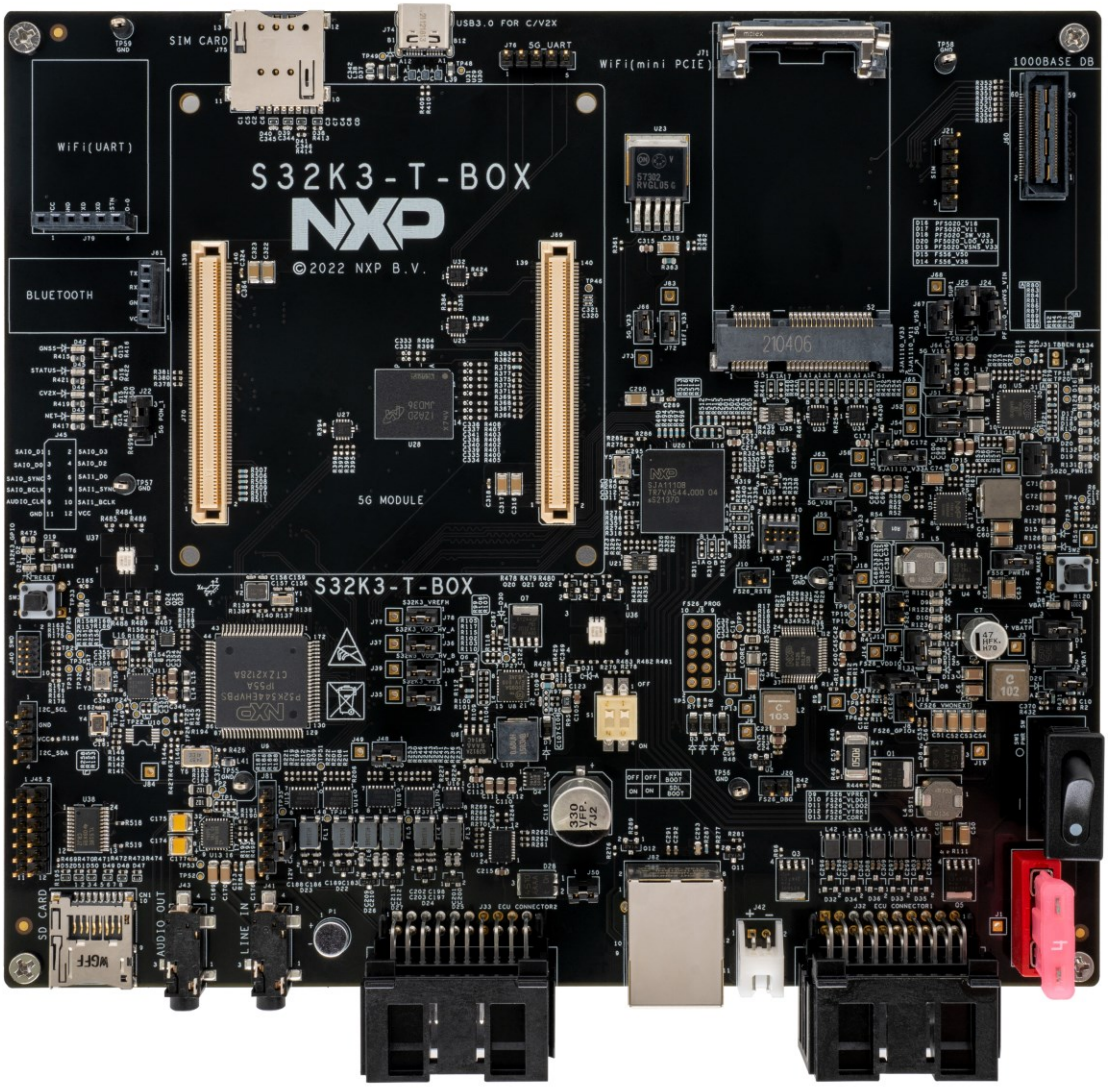
S32K3-T-BOX RDB
Hardware Reference Manual



Version: 0.5

Content

1.Introduction

The S32K3-T-BOX RDB is a compact, highly-optimized and integrated reference design board featuring the S32K3 general purpose microcontroller. This board can provide reference for a variety of typical automotive applications, such as 5G telematics box, service-oriented gateway, AVB, IO aggregator and body domain controller. It can be directly used by carmakers, suppliers and software ecosystem partners to accelerate development for shorter time-to-market.

This document describes the hardware features of the board specifications, block diagram, connectors and interfaces.

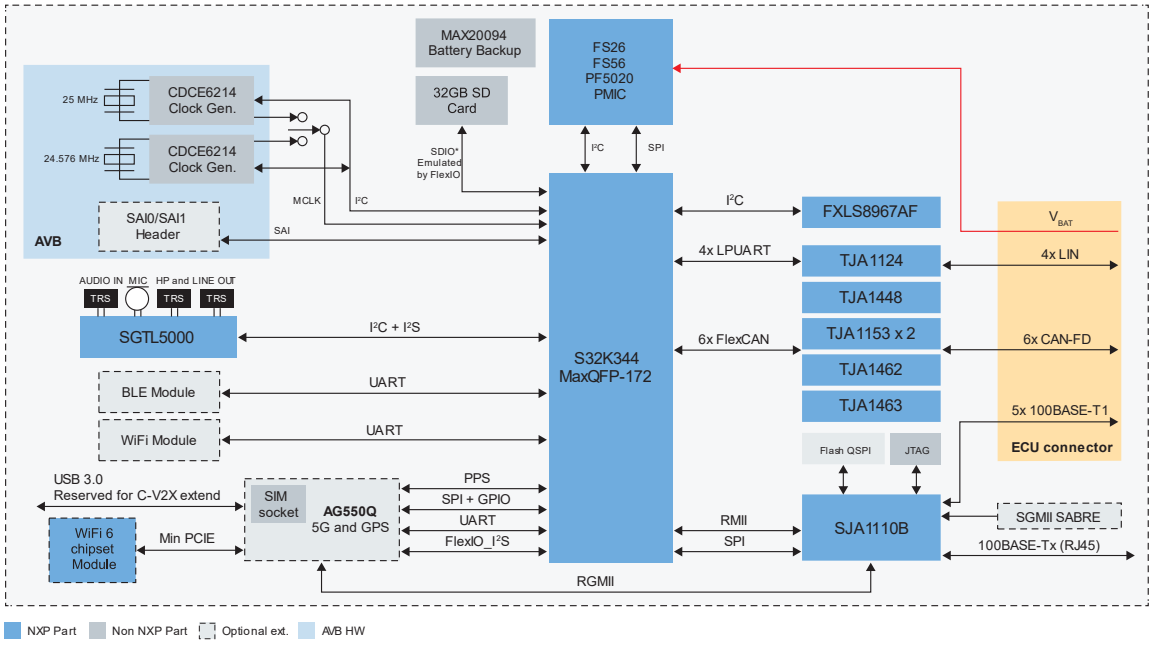


Figure 1. the Block Diagram of S32K3-T-BOX

2. Features Overview

- S32K344 maxQFP172 automotive microcontroller which integrates Arm cortex-M7 lockstep core, features hardware security engine(HSE) and supports ASIL D functional safety.
- Ethernet switch SJA1110B which integrates 5 channel 100base T1, 1 channel 100base Tx, 1 channel 1GHZ SGMII SABRE connector, with RMII connection to S32K3, RGMII connection to 5G module.
- Safety SBC FS26 supplying power for S32K3 and monitoring MCU status. PMIC FS56 and PF5020 providing additional power sources for the 5G module, ethernet switch and other peripherals.
- Automotive Grade Quectel 5G module AG55xQ designed with Qualcomm SA515M chip, with C-V2X and GNSS support.(Need to buy from the vender Quectel)
- WIFI 6 support with miniPCIE interface. Verified with NXP new generation WIFI6 chip AW690.
- 6 channel CAN FD and 4 channel LIN support which can be used for gateway application.
- Audio Codec SGTL5000 and clock multiplier CS2100 and CDCE6214 for AVB support.
- E-Call support with 3.0-7.0V backup battery charger and booster controller MAX20095.
- Automotive grade accelerometer FXLS8967AF to monitor vehicle status.
- A maxim 32GB SD Card can be implemented to store the vehicle data. The SDIO protocol is emulated by FLEXIO.

3. Power Supply

The S32K3-T-BOX RDB supports maxim 28V input voltage. Below is the power diagram.

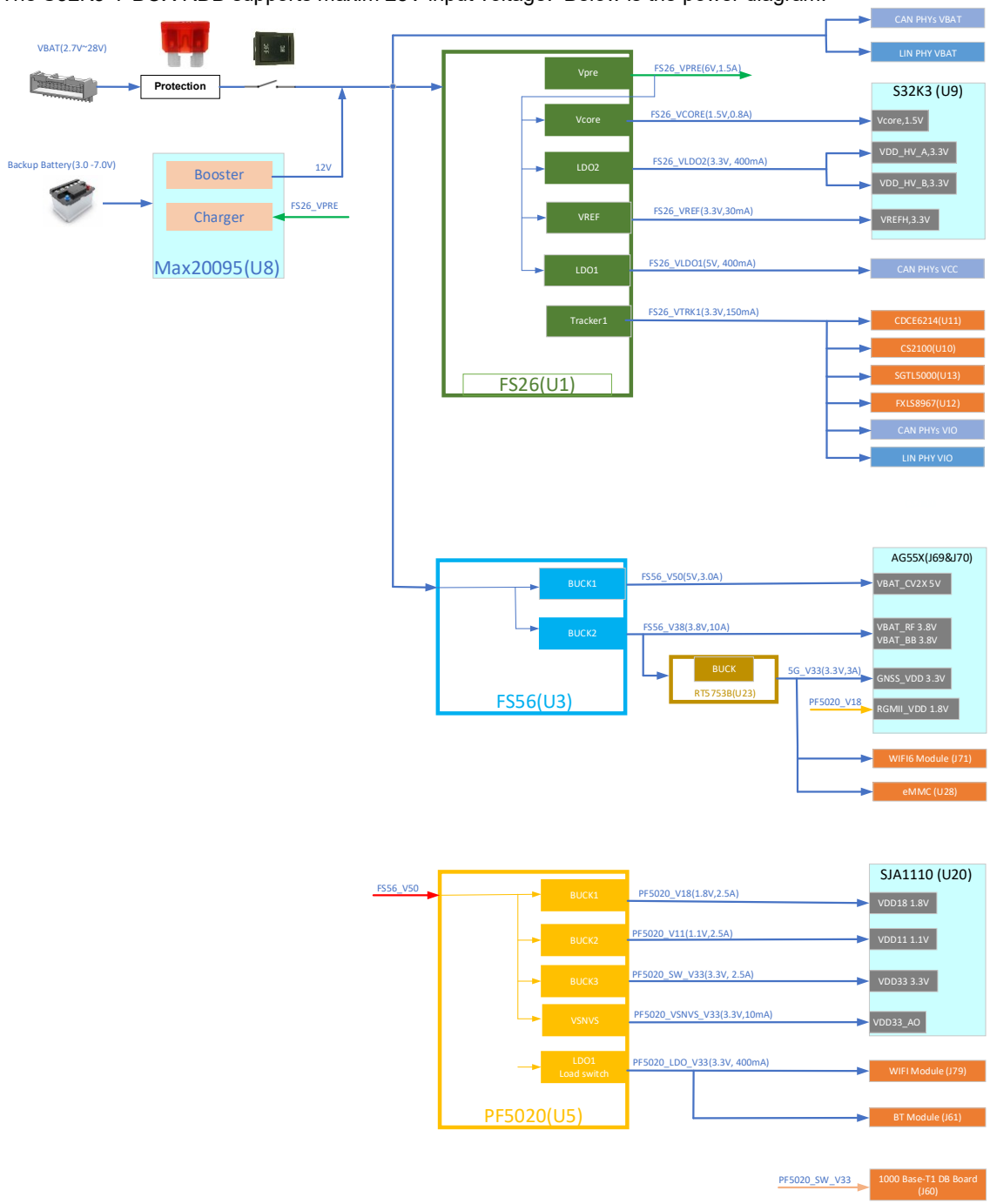
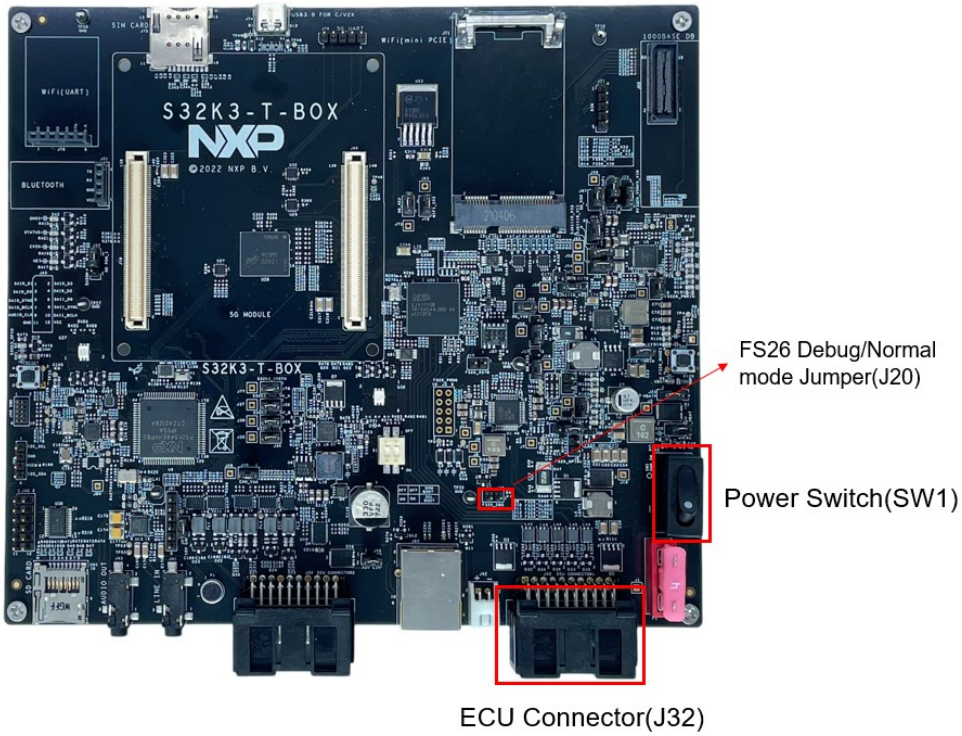


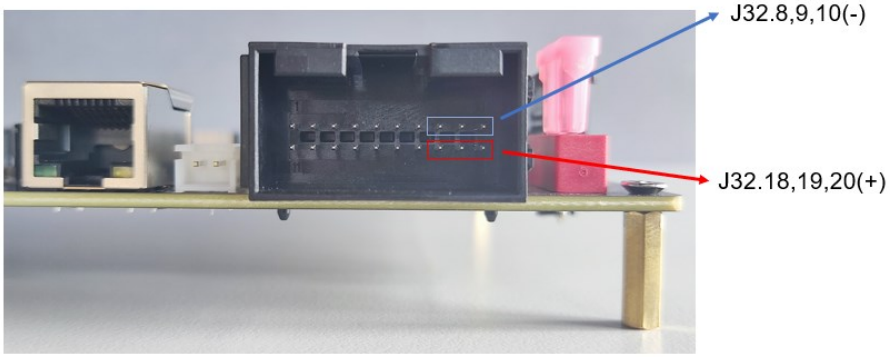
Figure 2. the Power Diagram

Please follow below sequence to power up the device.

1. Make sure the Jumper J20 is on.
2. Power the board through the ECU Connector J32.
3. Switch on the Power Switch SW1.



This is the connection for the main power from the ECU Connector J32.



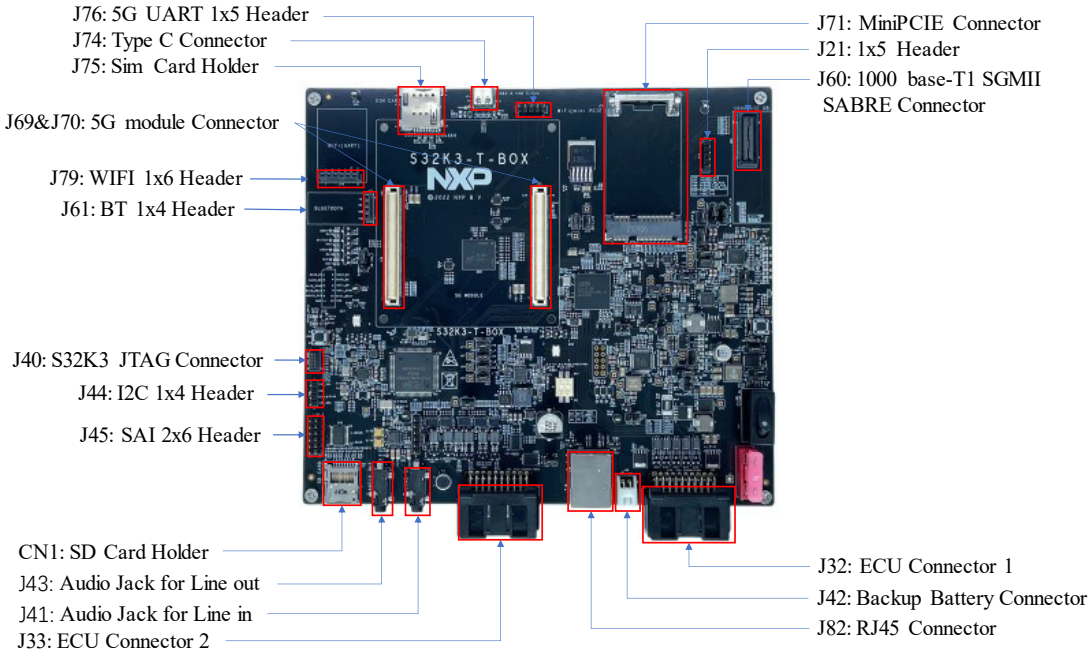
Note: Putting the Jumper J20 on is to supply voltage for the FS26 Debug pin before the VSUP is supplied, thus the FS26 can enter Debug mode. The Debug mode are intended for use during the engineering development process and not in the production application condition or in the vehicle. The watchdog and other failsafe function are disabled in the Debug mode. If you expect the FS26 to work in normal mode, the power up sequence is not required.

4. Connectors and interface

Table 1. the Connectors

Connectors	Function	Description
CN1	SD Card Holder	Connect to the SD card.
J21	1x5 Header	Unused GPIO pins of S32K3.
J32	ECU Connector 1	Connect to the 5 channel 100base-T1 ethernet interface, 12V main power supply input(J32.18,19,20) and the 4.2V backup battery input(J32.11,12).
J33	ECU Connector 2	Connect to the 6 channel CAN (FD) bus and 4 channel LIN bus.
J40	S32K3 JTAG Connector	2x5 10pin JTAG Connector for S32K3.
J41	Audio Jack for Line in	Connect to the microphone as the audio input for the codec.
J42	Backup Battery Connector	Connect to the 4.2V backup battery(The same as J32.11,12).
J43	Audio Jack for Line out	Connect to the headphone as the audio output for the codec.
J44	I2C 1x4 Header	J44 and J45 are together to connect to the external audio amplifier TDF8532 RDB board for AVB application.
J45	SAI 2x6 Header	J44 and J45 are together to connect to the external audio amplifier TDF8532 RDB board for AVB application.
J57	SJA1110 JTAG Connector	2x5 10 pin JTAG Connector for SJA1110.
J60	1000 base-T1 SGMII SABRE Connector	Connect to the external 1000 base-T1 ethernet PHY transceiver daughter board with SGMII interface, such as TJA1120.
J61	BT 1x4 Header	Connect to the Blue Tooth module HC08 with LPUART9.
J69 & J70	5G module Connector	Connect to the Quectel A55xQ 5G module.
J71	MiniPCIE Connector	Connect to the miniPCIE interface WIFI6 module. Recommend to use AW690 which has been verified by software.
J74	Type C Connector	This Type C connector is to communicate with the 5G module for V2X function.
J75	Sim Card Holder	Connect to the Sim card for 5G module.
J76	5G UART 1x5 Header	Connect to the PC with UART interface to interactive with the 5G module and print logs.
J79	WIFI 1x6 Header	Connect to the WIFI module ESP8266 with LPUART0.
J82	RJ45 Connector	Connect to the RJ45 industrial ethernet cable.

Below is the layout of these connectors.



This is the detail definition of the ECU Connectors.

CAN4_H	CAN4_L
CAN5_H	CAN5_H
CAN2_H	CAN2_H
CAN0_H	CAN0_H
CAN1_H	CAN1_H
CAN3_H	CAN3_H
GND	**GND**
LIN1	LIN3
VLIN	**VLIN**
LIN2	LIN4

J33 ECU Connector2

GND	**VBBAT**
GND	**VBBAT**
100BT1_5_P	100BT1_5_N
100BT1_6_P	100BT1_6_P
100BT1_7_P	100BT1_7_P
100BT1_8_P	100BT1_8_P
100BT1_9_P	100BT1_9_P
GND	**VBAT**
GND	**VBAT**
GND	**VBAT**

J32 ECU Connector1

5. Jumper Settings

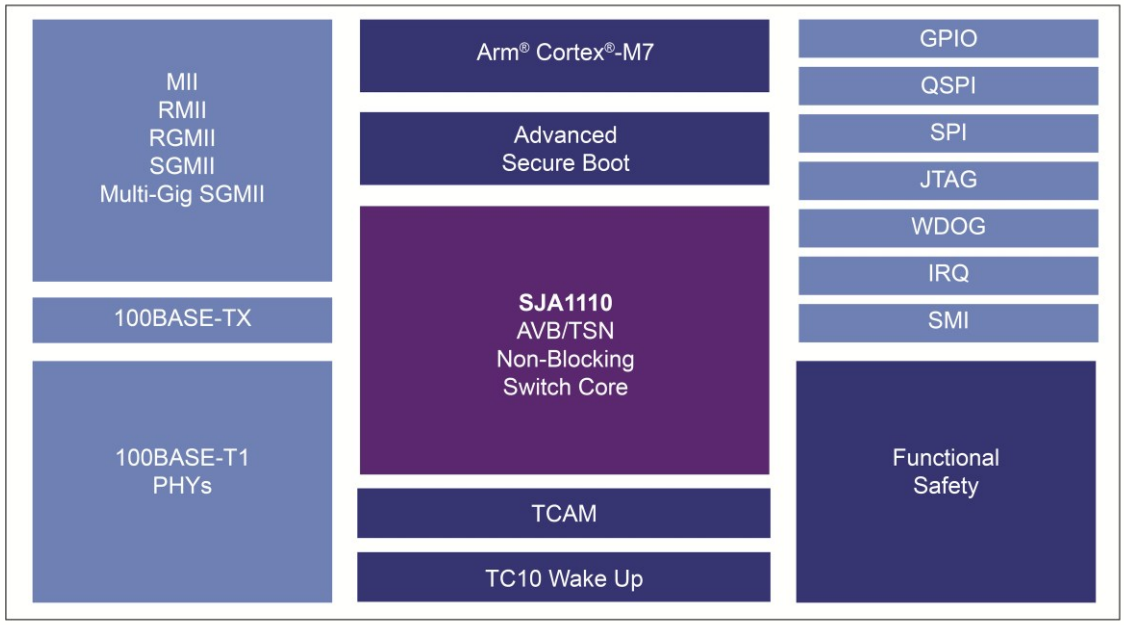
Table 2. the Jumpers

Jumper	Type	Default Setting	Description
J2	2 pins	Closed	The connection between VIN and VBAT, can be used for current monitoring.
J10	2 pins	Open	The connection between FS26 reset pin and S32K3 reset pin.
J15	2 pins	Closed	Use FS26_VLDO2(3.3V) as the I/O input supply of FS26.
J16	3 pins	1-2 Closed	1-2 Closed: FS26 monitors the FS26_VLDO1. 2-3 Closed: FS26 monitors the FS26_VLDO2.
J17	3 pins	1-2 Closed	1-2 Closed: FS26_VTRK1 is used as the input for BB_V33. 2-3 Closed: PF5020_LDO_V33 is used as the input for BB_V33.
J20	2 pins	1-2 Closed	Closed: FS26 will enter debug mode. Open: FS26 will enter normal mode.
J23	3 pins	2-3 Closed	1-2 Closed: Backup battery boost output VBATP is connected to VBAT thus the CAN and LIN PHY can be powered when the main power VIN is lost. 2-3 Closed: Backup battery boost output VBATP is connected to FS26_VPI thus the CAN and LIN PHY can not be powered when the main power VIN is lost.
J25	3 pins	1-2 Closed	1-2 Closed: Choose FS26_VPRE as the charging power source of the backup battery. 2-3 Closed: Choose FS56_V50 as the charging power source of the backup battery.
J27	2 pins	1-2 Closed	The connection between main power source and the power input of the PMIC FS56.
J30	2 pins	1-2 Closed	The connection between FS56_V50 and the power input of the PMIC PF5020.
J34	2 pins	1-2 Closed	The connection between FS26 VCORE and the S32K3 1.5V power supply.
J36	2 pins	1-2 Closed	The connection between FS26 LDO2 3.3V output and the S32K3 VDD_HV_A power supply.
J38	2 pins	1-2 Closed	The connection between FS26 LDO2 3.3V output and the S32K3 VDD_HV_B power supply.
J47	2 pins	1-2 Closed	The connection between the main power source and the battery supply voltage of the CAN PHYs.
J48	2 pins	1-2 Closed	The connection between FS26 LDO1 5V output and the 5V voltage supply of the CAN PHYs.
J50	2 pins	1-2 Closed	The connection between the main power source and the battery supply voltage of the LIN PHY.
J51	2 pins	1-2 Closed	The connection between the PF5020 1.1V output and the SJA1110 1.1V power supply.

J53	2 pins	1-2 Closed	The connection between the PF5020 3.3V output and the SJA1110 3.3V power supply.
J55	3 pins	1-2 Closed	1-2 Closed: Choose the output of the LDO RT9058 as the SJA1110 3.3V AO(Always On) power supply. 2-3 Closed: Choose PF5020 VSNVS 3.3V output as the SJA1110 3.3V AO(Always On) power supply.
J58	3 pins	1-2 Closed	1-2 Closed: Choose the PF5020 LDO1OUT 3.3V as the DB_V33 power supply. 2-3 Closed: Choose the PF5020 BUCK3 3.3V as the DB_V33 power supply.
J62	3 pins	1-2 Closed	The connection between FS56 SW2 3.8V and the VBAT_BB, VBAT_RF of the 5G module.
J64	2 pins	1-2 Closed	The connection between FS5020 SW1 1.8V and the RGMII_VDD of the 5G module.
J66	2 pins	1-2 Closed	Use the 5G_V38 as the input of the LDO NCV57302 to generate 5G_V33 which will power the GNSS in the 5G module, miniPCIE WIFI6 module and eMMC.
J67	2 pins	1-2 Closed	The connection between FS56 SW1 5V and the VBAT_CV2X of the 5G module.
J72	2 pins	1-2 Closed	The connection between 5G_V33 and the power supply of the miniPCIE WIFI module.
J78	2 pins	1-2 Closed	The connection between FS26 VREF and the S32K3 VREFH.

6. Automotive Ethernet Switch

The S32K3-T-BOX RDB has an automotive TSN Ethernet switch SJA1110B which mainly comprises of a configurable Ethernet switch and a programmable Arm Cortex-M7 core. It also supports advanced secure boot capability.



The QuadSPI port is connected to an external flash, the SPI_HOST interface is connected to the S32K3. The SJA1110 can be booted from the external flash(NVM Boot) or S32K3(SDL Boot) . When there is no firmware in the external flash, it will switch to SDL Boot mode automatically.

An SABRE connector with SGMII interface is designed to connect the NXP 1GHZ automotive ethernet PHY TJA1120 daughter board.

More details please check the document “SJA1110 Automotive Ethernet User Switch.pdf” .

This is the SJA1110B diagram in S32K3-T-BOX RDB.

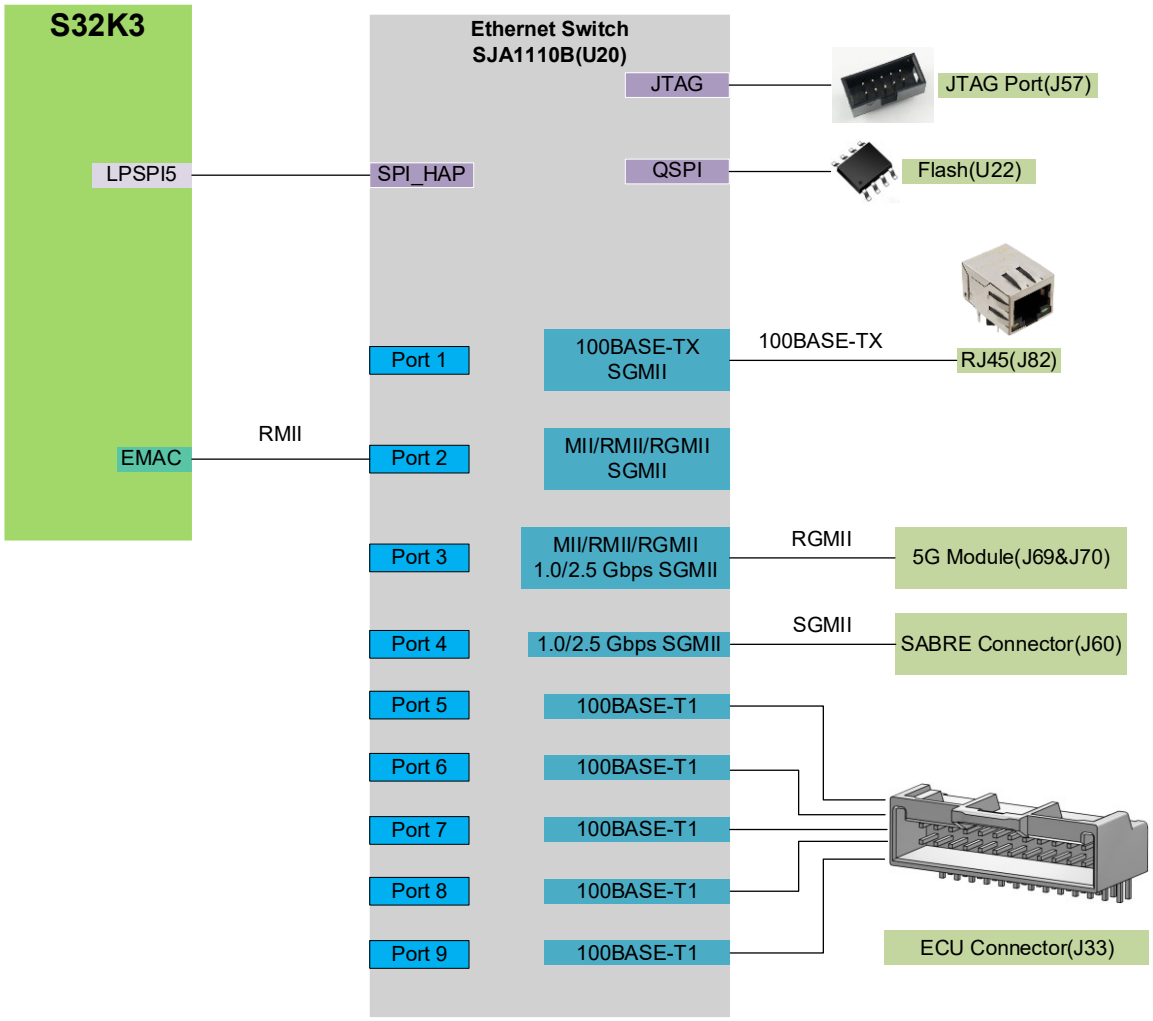
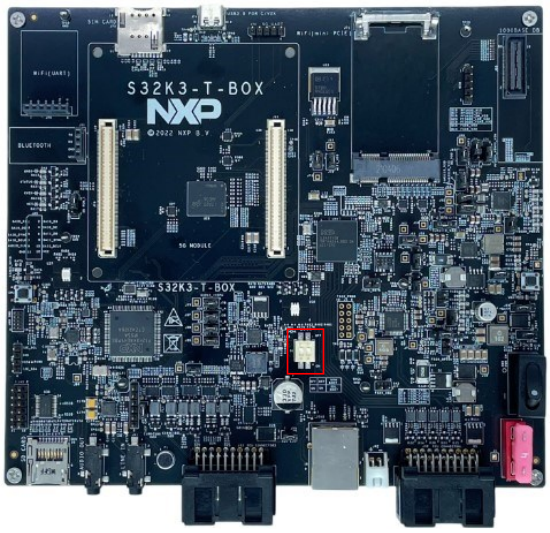
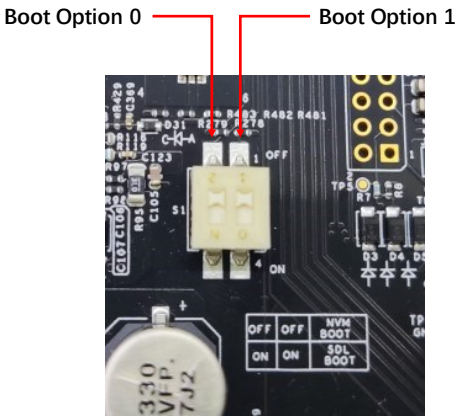


Figure3. the Ethernet Switch SJA1110B Block Diagram

On S32K3-T-BOX RDB board, the boot mode of SJA1110B can be chosen by setting the 2 boot option pins on the dial switch S1.





Below is the Boot options of SJA1110B.

Table 3. SJA1110B Boot Options

Boot Option 0	Boot Option 1	Boot Mode
OFF	OFF	NVM Boot
ON	ON	SDL Boot

Below is the full connection of the Ethernet port on SJA1110B.

Table 4. SJA1110B Ethernet Port Connections

SJA1110 Ethernet Port	Function	Connection
P1	100 Base-TX	RJ45 Connector
P2	RMII	S32K3
P3	RGMII	5G Module
P4	SGMII	SABRE Connector
P5	100 Base-T1	ECU Connector J32.Pin3,13
P6	100 Base-T1	ECU Connector J32.Pin4,14
P7	100 Base-T1	ECU Connector J32.Pin5,15
P8	100 Base-T1	ECU Connector J32.Pin6,16
P9	100 Base-T1	ECU Connector J32.Pin7,17

7.5G Module

S32K3-T-BOX RDB has a 5G module AG55xQ from Quectel which supports C-V2X function and GNSS location.

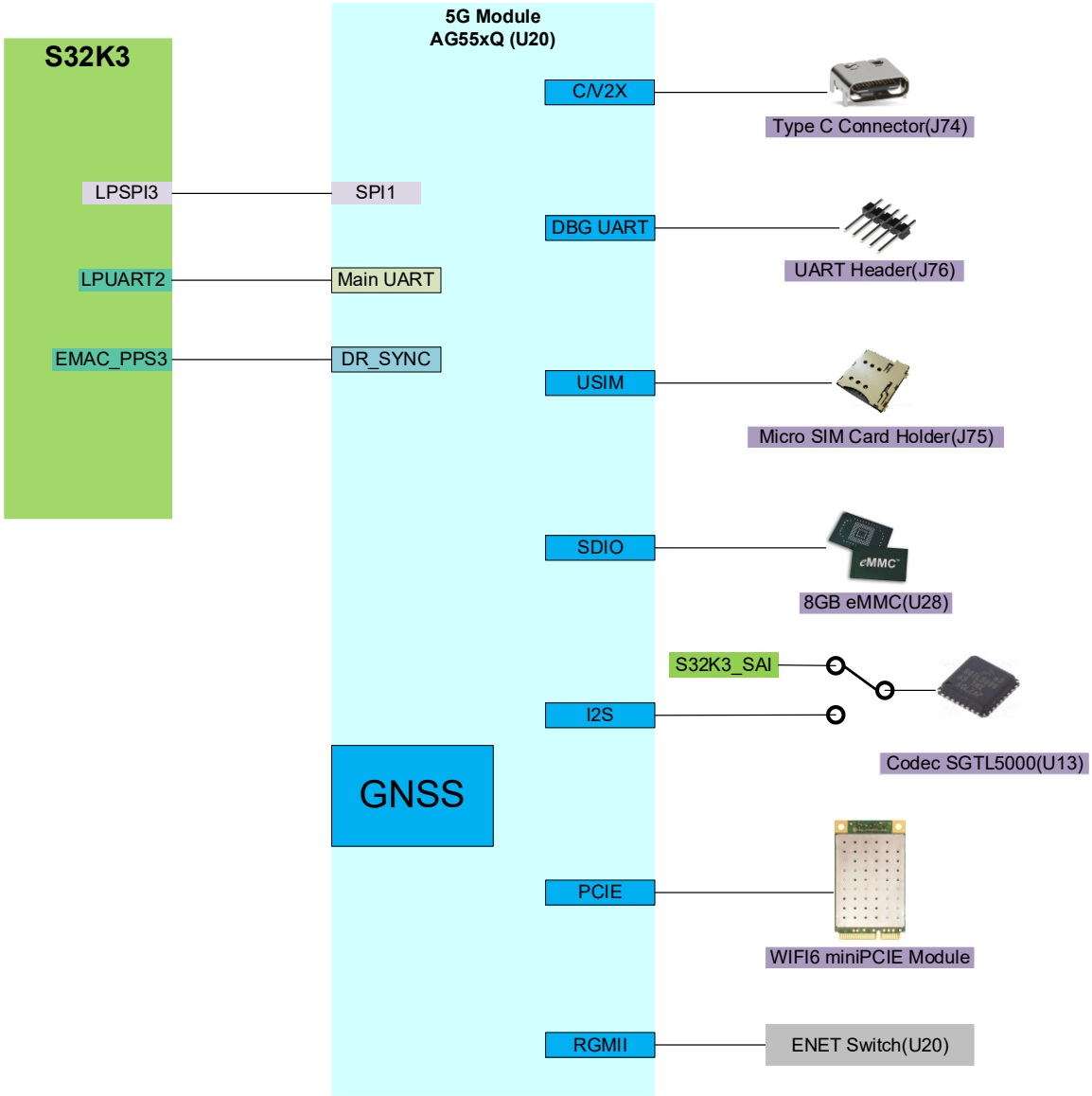


Figure4. the 5G Module Diagram

This module supports both 5G NR NSA and SA modes. Adopting 3GPP Rel-15 technology, the module supports maximum 2.4 Gbps downlink and 550 Mbps uplink data rates at 5G NSA mode, and maximum 1.6 Gbps downlink and 200 Mbps uplink data rates at LTE-A. More detail please check the datasheet of AG55xQ.

J74 Type C connector is for C/V2X communication, J76 1x5 UART Header is to Connect to the PC to interactive with the 5G module and print logs.

An 8GB eMMC is designed to store the code, configuration file and other user information .etc.

The 5G module can interact with S32K3 by SPI and UART interface, and connect with the ethernet switch with an RGMII interface.

The 5G module can connect to the codec SGTL5000 with I2S interface by controlling the multiplexer-demultiplexer TS3A27518E(U38) to realize the call function. User can insert a Micro sim card to activate the 5G communication.

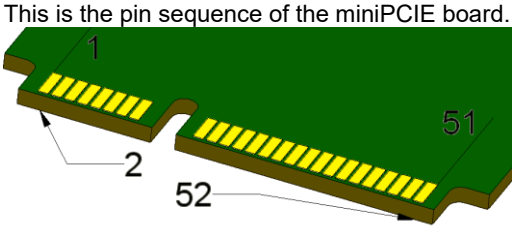
Since the IO voltage of the 5G module is 1.8V while S32K3 and most of the peripherals are 3.3V so the level shifters are used for these connections.

WIFI6 is supported and is connected with 5G module by miniPCIE interface. A miniPCIE connector is designed on this board and below is the PCIE pin definition. You can design your own WIFI6 miniPCIE board with the below miniPCIE pin definition. We suggest to use NXP product AW690 which is tested with S32K3-T-BOX RDB.

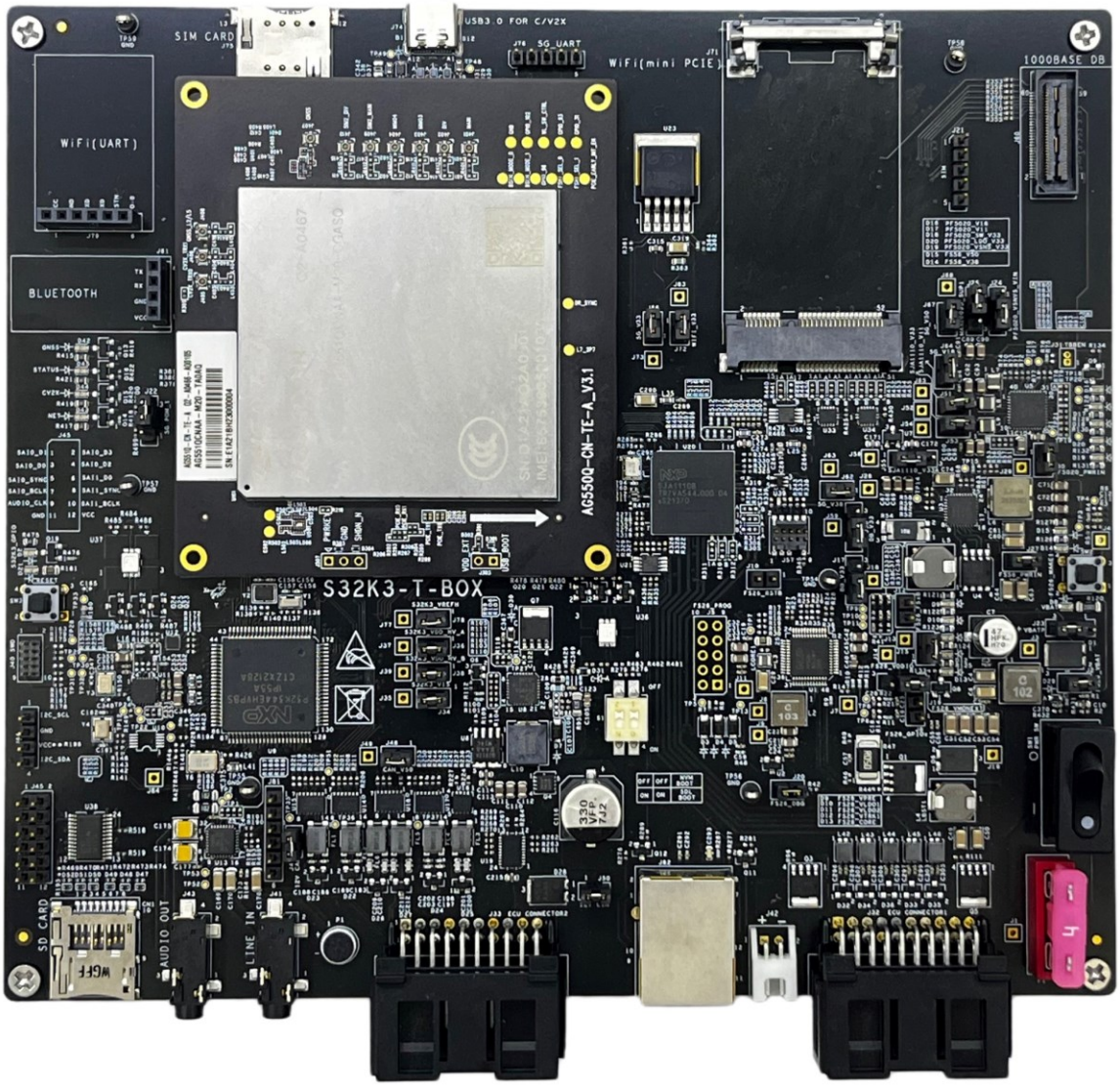
Table 5. the Definition of Supported miniPCIE WIFI6 Module

Pin Number	**Definition**	**Pin Number**	Definition
1	WAKE#	2	3.3V
3	Reserved	4	GND
5	Reserved	6	Reserved
7	CLKREQ#	8	Reserved
9	GND	10	Reserved
11	REFCLK-	12	Reserved
13	REFCLK+	14	Reserved
15	GND	16	Reserved
17	Reserved	18	GND
19	Reserved	20	Reserved
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux
25	PERp0	26	GND
27	GND	28	Reserved
29	GND	30	Reserved
31	PETn0	32	Reserved
33	PETp0	34	GND
35	GND	36	Reserved
37	Reserved	38	Reserved
39	5G_GPIO6	40	GND
41	5G_GPIO5	42	Reserved
43	5G_BT_EN	44	Reserved
45	5G_BT_UART_RTS	46	Reserved
47	5G_BT_UART_TXD	48	Reserved
49	5G_BT_UART_RXD	50	GND
51	5G_BT_UART_CTS	52	+3.3V

This is the pin sequence of the miniPCIE board.



Below is the picture when 5G module is put on the S32K3-T-BOX RDB board.



8.AVB Hardware

S32K3-T-BOX RDB features the Ethernet AVB related hardware, which includes the 2 media clock generators CS2100(U10) , CDCE6214(U11) and a codec SGTL5000(U13).

The I2S interface of the codec is connected to S32K3 for AVB application by default.

An SAI(J45) interface is extended out for external audio amplifier board, such as the NXP automotive Class-D TDF853x RDB board.

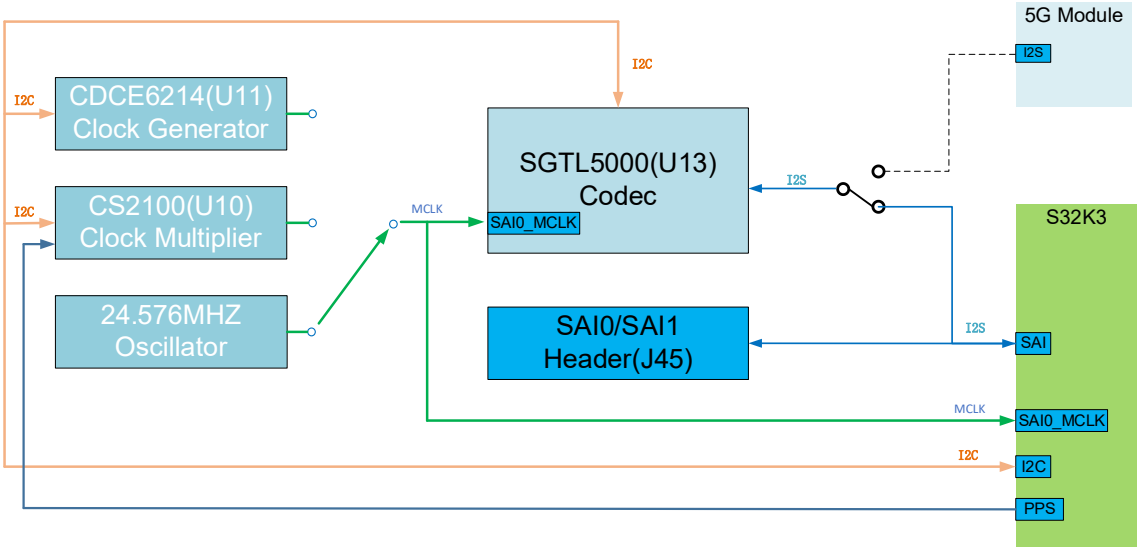


Figure5. the AVB Hardware Diagram

9. Backup Battery E-Call Support

S32K3-T-BOX RDB integrated a backup battery charger and boost controller chip MAX20095.

When the main power is lost, it can boost the battery to 12V to support the emergency call function. When the main power is on, the chip works as a charger for the battery.

The MAX20095 can be controlled by S32K3 through I2C interface. The charger voltage can be set to 3.0 – 7.0V. Default value is 3.6V. The current can be set up to 1A.

If you want to power the CAN &LIN PHYs using backup battery, switch the jumper J23 to 1-2 on. You can connect the battery to J42 or J32.

For more detail please check the datasheet of MAX20095.

10. Others

An accelerometer FXLS8967(U12) is integrated to detect the speed of the car.

A header(J61) is designed for connecting the HC-08 bluetooth module.

Header(J79) is designed for connecting the ATK-ESP8266 WIFI module.

An SD card can be inserted to store the data. The SDIO protocol is simulated by FLEXIO and controlled by S32K3.

11. Abbreviations Used in the Document

Abbreviation	Description
T-Box	Telematics Box
AVB	Audio Video Bridging
NVM	Non-volatile Memory
SDL	Serial DownLoad
SBC	System Basic Chip
PMIC	Power Management IC
HSE	Hardware Security Engine
E-Call	Emergency Call
GNSS	Global Navigation Satellite System
eMMC	Embedded Multimedia Card
PHY	Physical Layer
RGMII	Reduced General Media Independent Interface
SGMII	Serial Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
MII	Media Independent Interface

12. Revision History

Date	Version	Description
29th Apr, 2022	0.1	Initial Draft
13th May, 2022	0.2	Uploaded the diagrams and pictures
24th June,2022	0.3	changed the block diagram with NXP and none NXP part
27th July,2022	0.4	Updated the new block diagram and board picture
1st August,2022	0.5	Unified the font