



PSMN1R5-50YLH

N-channel 50 V, 1.7 mOhm, 200 A continuous, logic level
Application Specific MOSFET in LPAK56E

26 January 2022

Product data sheet

1. General description

200 Amp continuous current, logic level gate drive, N-channel enhancement mode MOSFET in LPAK56E package. Part of the ASFETs for Battery Isolation and DC Motor control family and using Nexperia's unique "SchottkyPlus" technology delivers high efficiency and low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. The ASFET is particularly suited to 36 V battery powered applications requiring strong avalanche capability, linear mode performance, use at high switching frequencies, and also safe and reliable switching at high load-current.

2. Features and benefits

- 200 A continuous current capability
- Optimised for 36 V (nominal) battery powered applications
- LPAK56E low-stress exposed lead-frame for ultimate reliability, optimum soldering and easy solder-joint inspection
- Copper-clip and solder die attach for low package inductance and resistance, and high I_D (max) rating
- Qualified to 175 °C
- Avalanche rated, 100% tested
- Low Q_G , Q_{GD} and Q_{OSS} for high efficiency, especially at higher switching frequencies
- Superfast switching with soft body-diode recovery for low-spiking and ringing, recommended for low EMI designs
- Unique "SchottkyPlus" technology for Schottky-like switching performance and low I_{DSS} leakage
- Narrow $V_{GS(th)}$ rating for easy paralleling and improved current sharing
- Very strong linear-mode / safe operating area characteristics for safe and reliable switching at high-current conditions

3. Applications

- Brushless DC motor control
- Synchronous rectifier in high-power AC-to-DC applications, e.g. server power supplies
- Battery protection and Battery Management Systems (BMS)
- Load switch
- 10 cell lithium-ion battery applications (36 V – 42 V)

4. Quick reference data

Table 1. Quick reference data

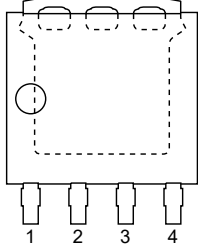
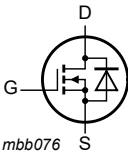
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	50	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	200	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	333	W
T_j	junction temperature			-55	-	175	°C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	1.4	1.75	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	1.6	2	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 25 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13		-	13	29	nC
Q _{G(tot)}	total gate charge			-	53	82	nC

[1] 200A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56E; Power-SO8 (SOT1023)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R5-50YLH	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R5-50YLH	1H550L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$	-	50	V
V_{DGR}	drain-gate voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	50	V

Symbol	Parameter	Conditions		Min	Max	Unit
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	333	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	200	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	200	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	1159	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C

Source-drain diode

I_S	source current	$T_{mb} = 25\text{ °C}$		-	200	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	1159	A

Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 50\text{ A}$; $V_{sup} \leq 50\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 513\text{ }\mu\text{s}$	[2]	-	833	mJ
		$I_D = 25\text{ A}$; $V_{sup} \leq 50\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 2.5\text{ ms}$	[2]	-	2	J
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[2]	-	115	A

- [1] 200A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

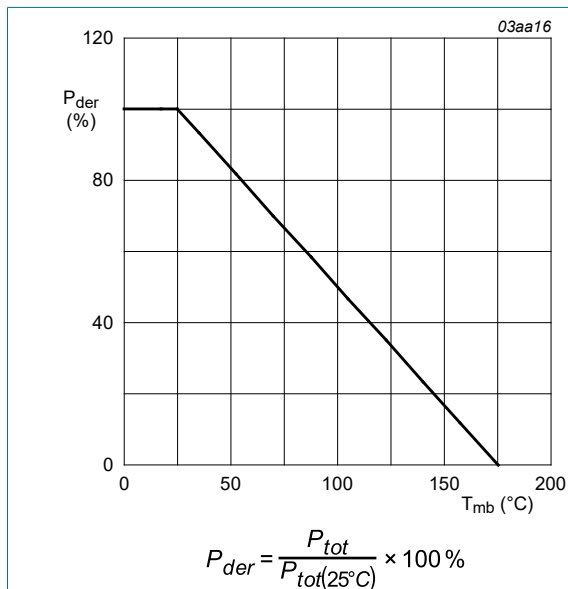
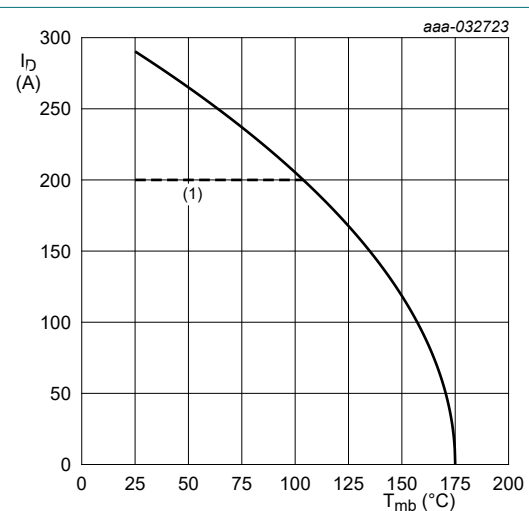


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

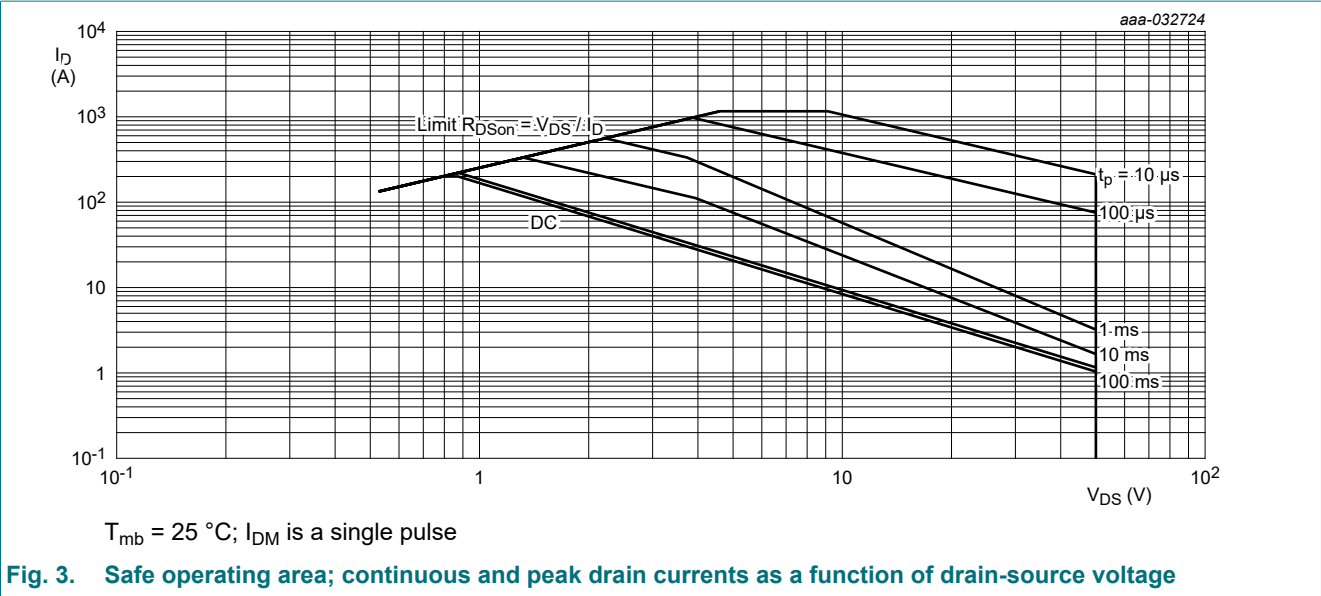


$V_{GS} \geq 10\text{ V}$

(1) 200A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

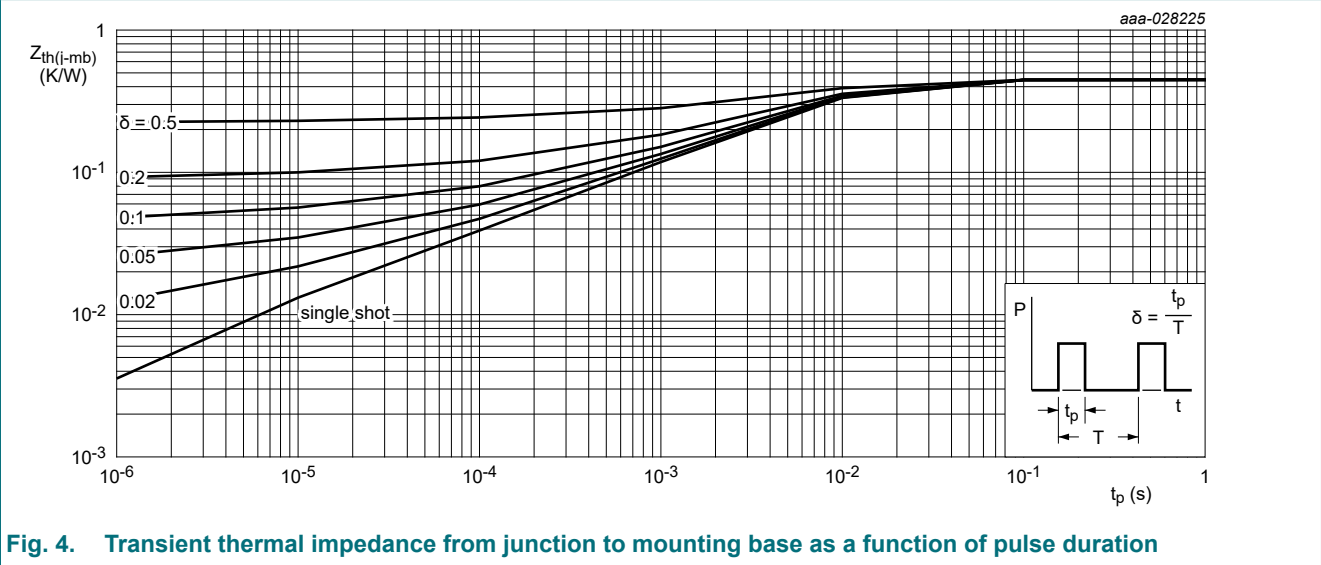
N-channel 50 V, 1.7 mOhm, 200 A continuous, logic level Application Specific MOSFET in LPAK56E

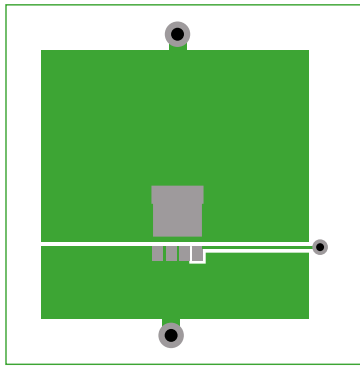


9. Thermal characteristics

Table 6. Thermal characteristics

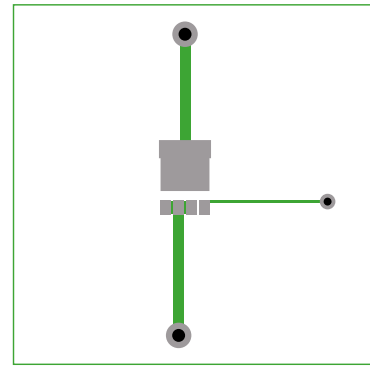
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.33	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	42	-	K/W
		Fig. 6	-	85	-	K/W





Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$	50	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^\circ C$	45	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 ^\circ C$	1.2	1.61	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 ^\circ C \leq T_j \leq 150 ^\circ C$	-	-4.6	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 ^\circ C$	-	0.01	1	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 125 ^\circ C$	-	3.9	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 ^\circ C$; Fig. 10	-	1.4	1.75	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 150 ^\circ C$; Fig. 11	-	-	3.52	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 ^\circ C$; Fig. 10	-	1.6	2	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 ^\circ C$; Fig. 11	-	-	4.02	mΩ
R_G	gate resistance	$f = 1 MHz; T_j = 25 ^\circ C$	0.52	1.3	3.3	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 25 V; V_{GS} = 4.5 V$; Fig. 12 ; Fig. 13	-	53	82	nC
		$I_D = 25 A; V_{DS} = 25 V; V_{GS} = 10 V$; Fig. 12 ; Fig. 13	-	117	181	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	61	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 25\text{ A}$; $V_{DS} = 25\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 12 ; Fig. 13		-	17	26	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	11.3	17	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	5.4	8	nC
Q_{GD}	gate-drain charge			-	13	29	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 25\text{ V}$; Fig. 12 ; Fig. 13		-	2.5	-	V
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 14		-	7959	11143	pF
C_{oss}	output capacitance			-	799	1119	pF
C_{rss}	reverse transfer capacitance			-	231	554	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 25\text{ V}$; $R_L = 1\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$		-	39	-	ns
t_r	rise time			-	40	-	ns
$t_{d(off)}$	turn-off delay time			-	68	-	ns
t_f	fall time			-	32	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$		-	42	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 15		-	0.75	1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; Fig. 16		-	36	-	ns
Q_r	recovered charge		[1]	-	37	-	nC
t_a	reverse recovery rise time			-	21	-	ns
t_b	reverse recovery fall time			-	14	-	ns

[1] includes capacitive recovery

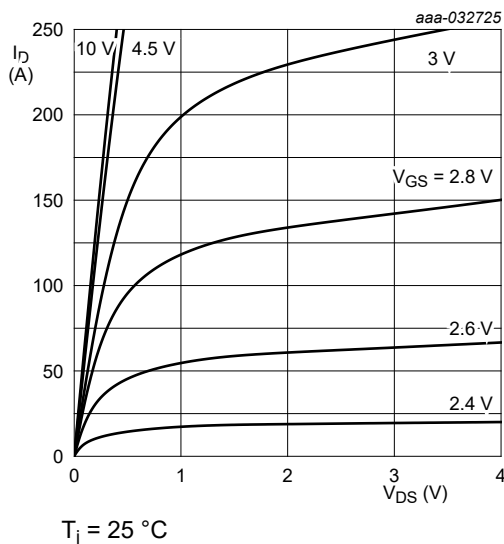


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

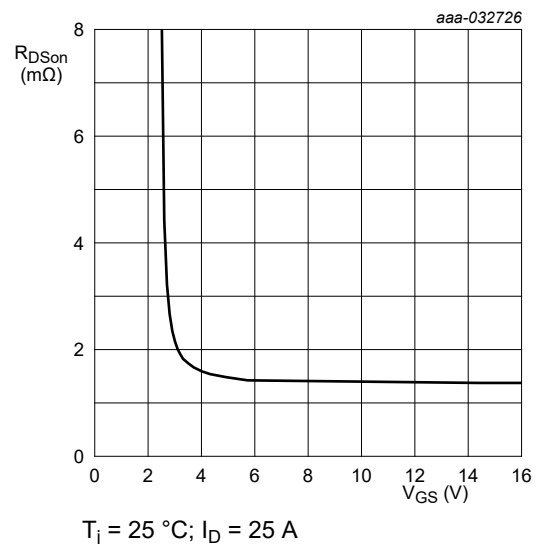


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

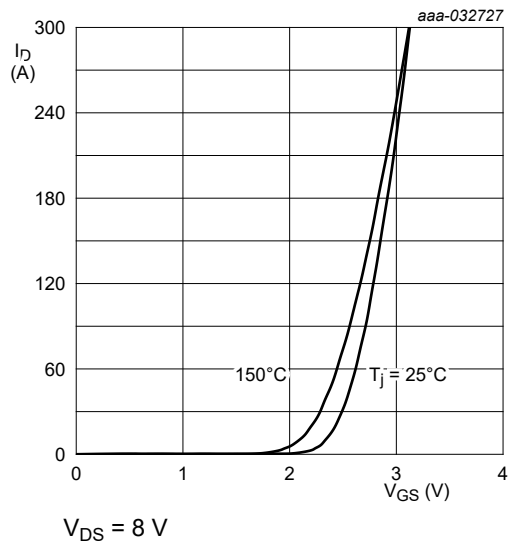


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

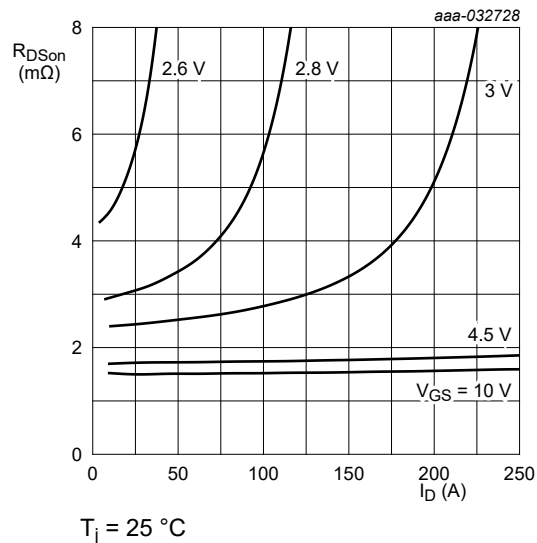


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

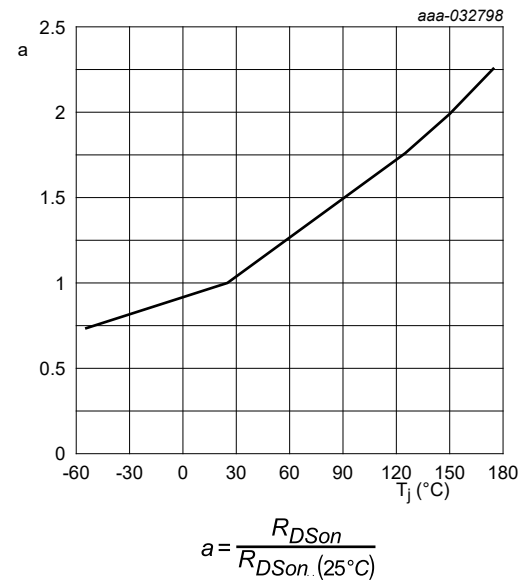


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

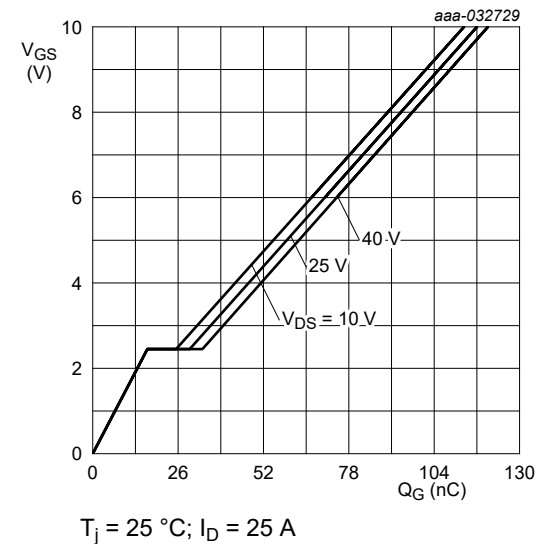


Fig. 12. Gate-source voltage as a function of gate charge; typical values

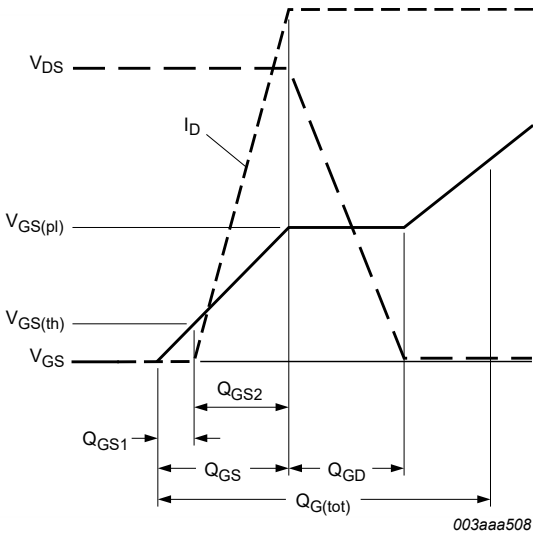


Fig. 13. Gate charge waveform definitions

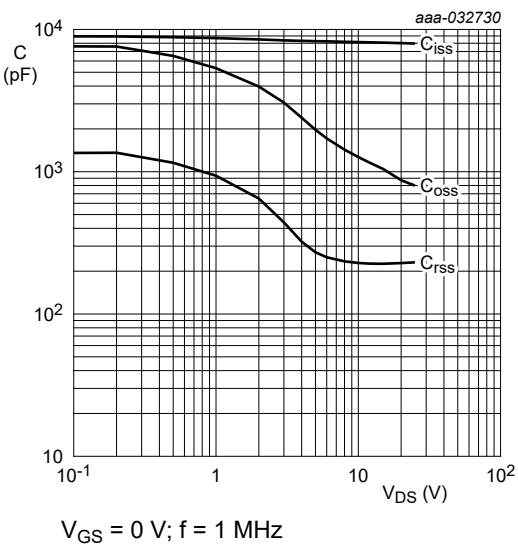


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

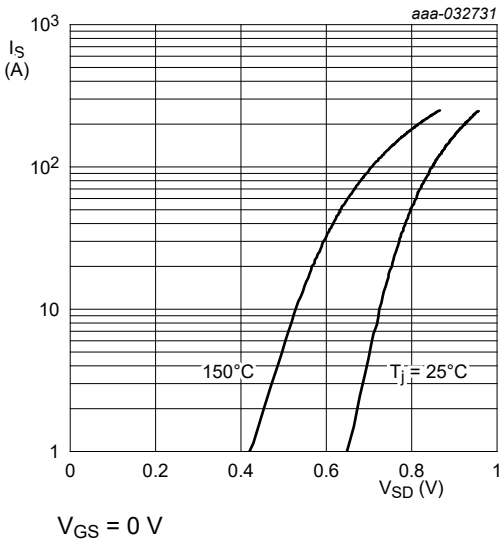


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

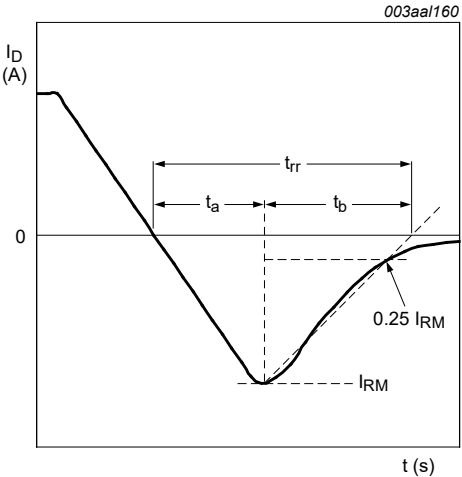


Fig. 16. Reverse recovery timing definition

11. Package outline

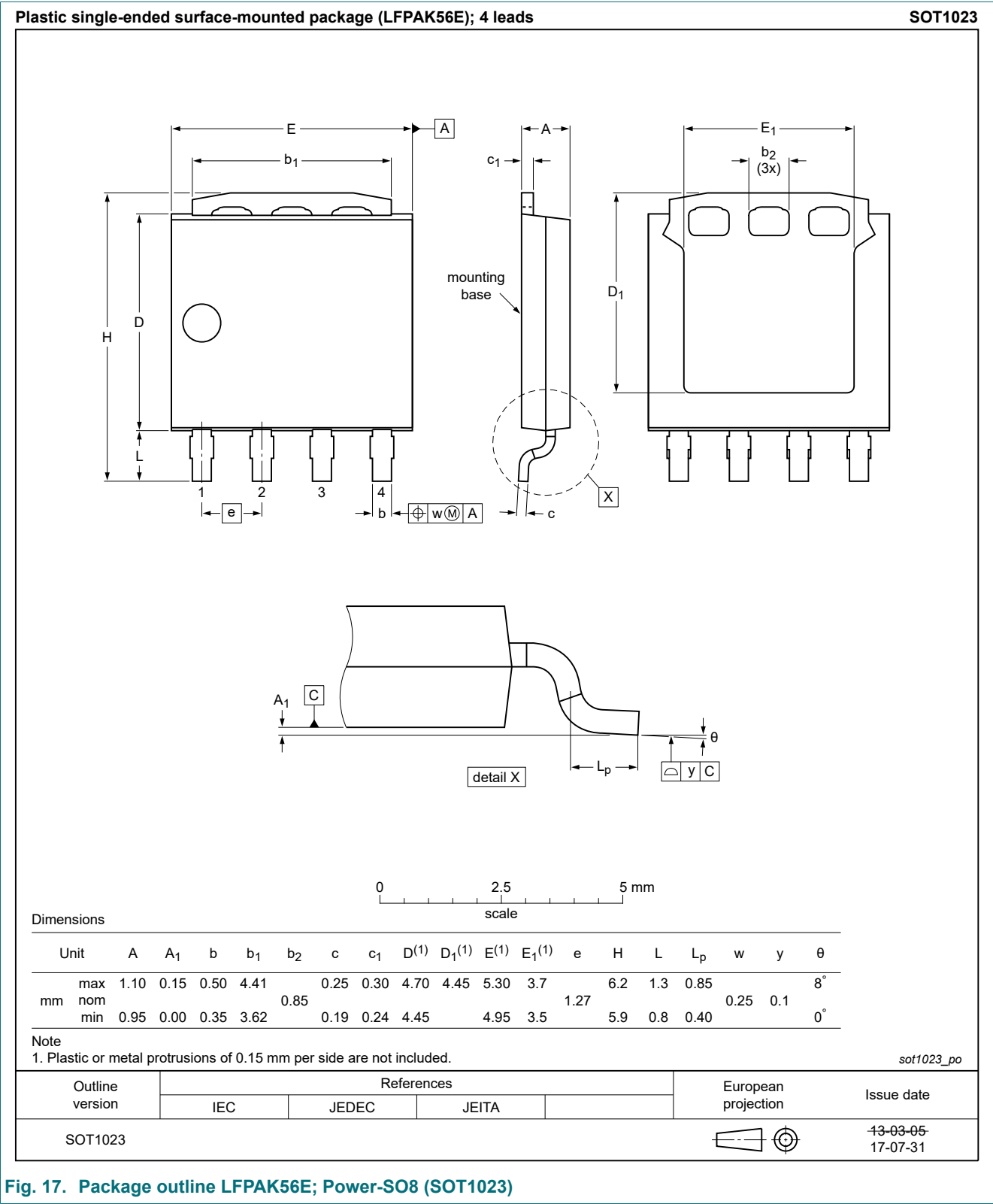


Fig. 17. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

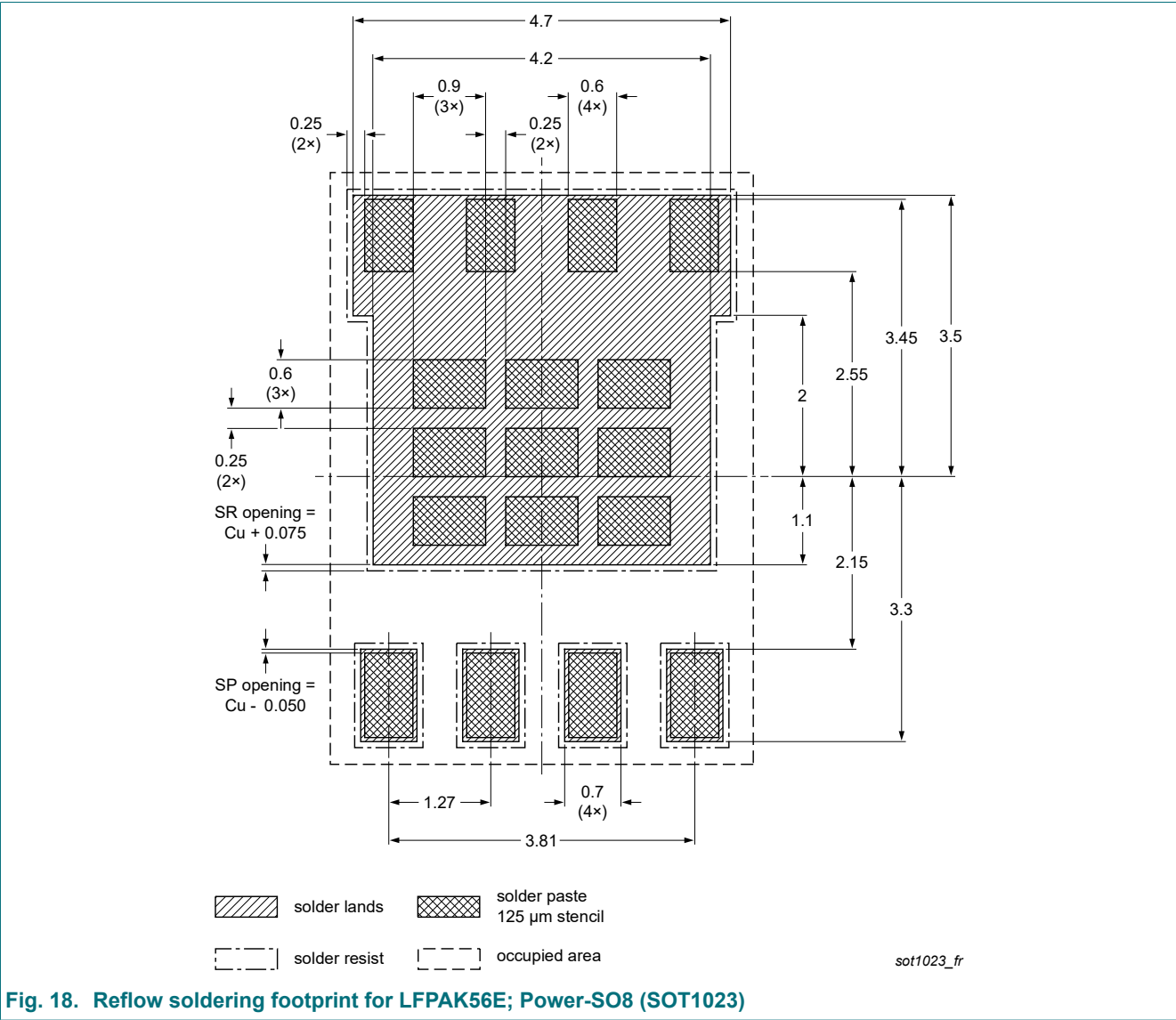


Fig. 18. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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