



PXN012-60QL

N-channel 60 V, 11.5 mOhm, logic level Trench MOSFET in MLPAK33

8 July 2021

Product data sheet

1. General description

General purpose, 42 A rated, logic level N-channel enhancement mode Power MOSFET in MLPAK33 package.

2. Features and benefits

- Logic level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Motor drive
- LED lighting
- Load switching
- Auxiliary control
- Fan control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C		-	-	60	V
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C; Fig. 2		-	-	42	A
P _{tot}	total power dissipation	T _{sp} = 25 °C; Fig. 1		-	-	34.7	W
T _j	junction temperature			-55	-	150	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 9		-	9.8	11.5	mΩ
		V _{GS} = 4.5 V; I _D = 10 A; T _j = 25 °C; Fig. 9		-	14	17.6	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 30 V; V _{GS} = 4.5 V; T _j = 25 °C; Fig. 11 ; Fig. 12		-	4.3	-	nC
Q _{G(tot)}	total gate charge			-	9.64	-	nC
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 3.5 A; T _{j(init)} = 25 °C; unclamped	[1]	-	-	90	mJ

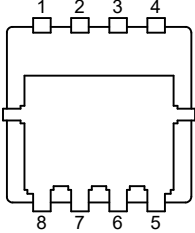
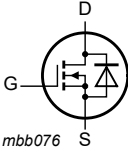
N-channel 60 V, 11.5 mOhm, logic level Trench MOSFET in MLPAK33

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q_r	recovered charge	$I_S = 10\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 15	[2]	-	13	-	nC

[1] Protected by 100% test
[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN012-60QL	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN012-60QL	7AB

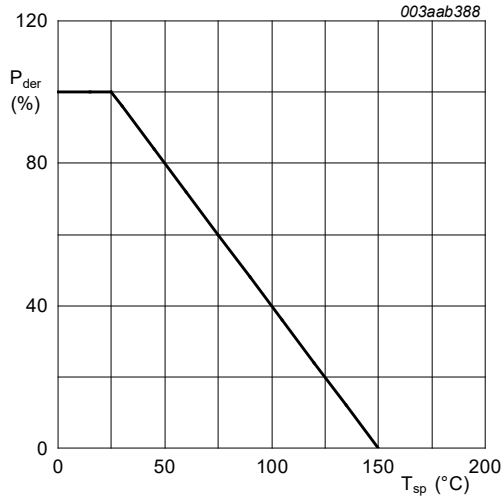
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

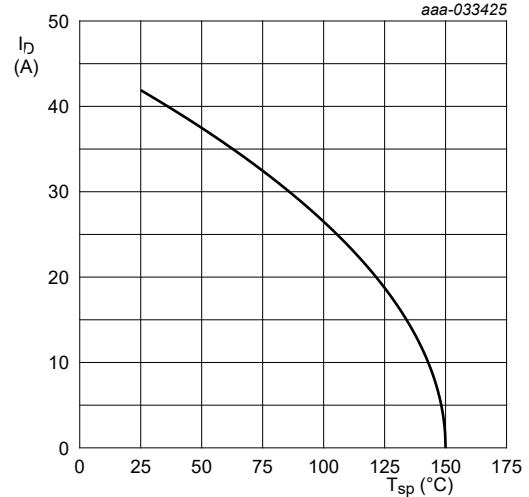
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 150\text{ °C}$	-	60	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Fig. 1	-	34.7	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{sp} = 25\text{ °C}$; Fig. 2	-	42	A
		$V_{GS} = 10\text{ V}$; $T_{sp} = 100\text{ °C}$; Fig. 2	-	26	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{sp} = 25\text{ °C}$; Fig. 3	-	168	A
T_{stg}	storage temperature		-55	150	°C
T_J	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	29	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{sp} = 25\text{ °C}$	-	168	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 3.5\text{ A}$; $T_{J(\text{init})} = 25\text{ °C}$; unclamped	[1]	-	90 mJ
I_{AS}	non-repetitive avalanche current	$T_{J(\text{init})} = 25\text{ °C}$	[1]	-	3.5 A

[1] Protected by 100% test



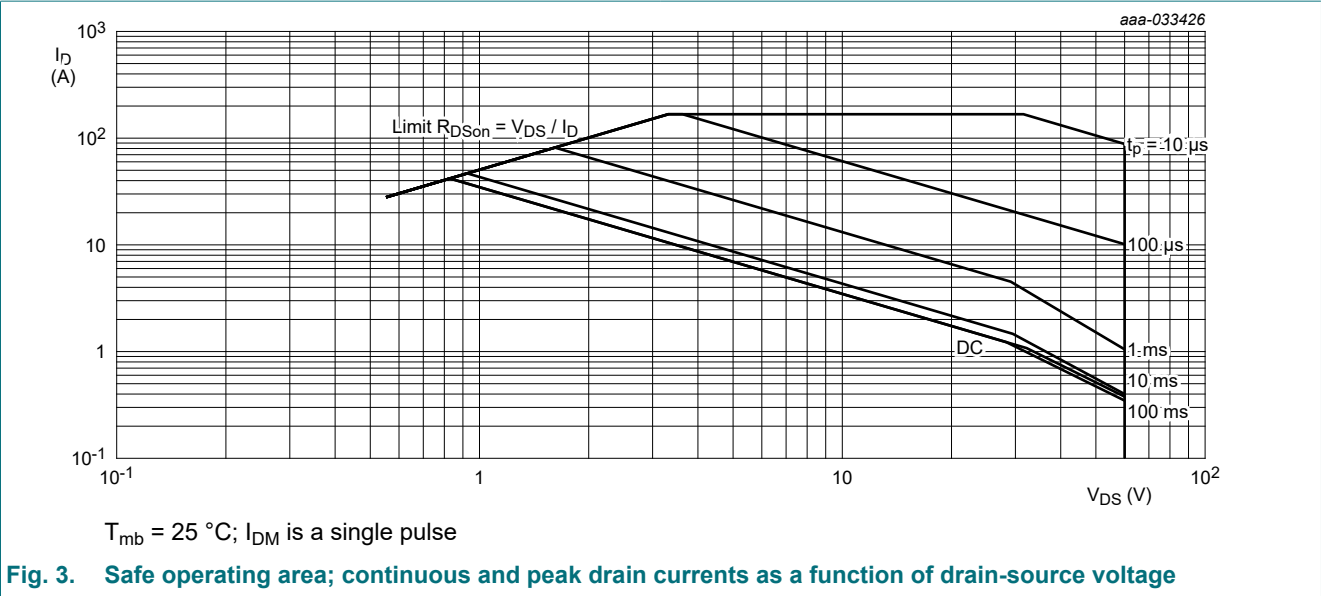
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of solder point temperature



$V_{GS} \geq 10\text{ V}$

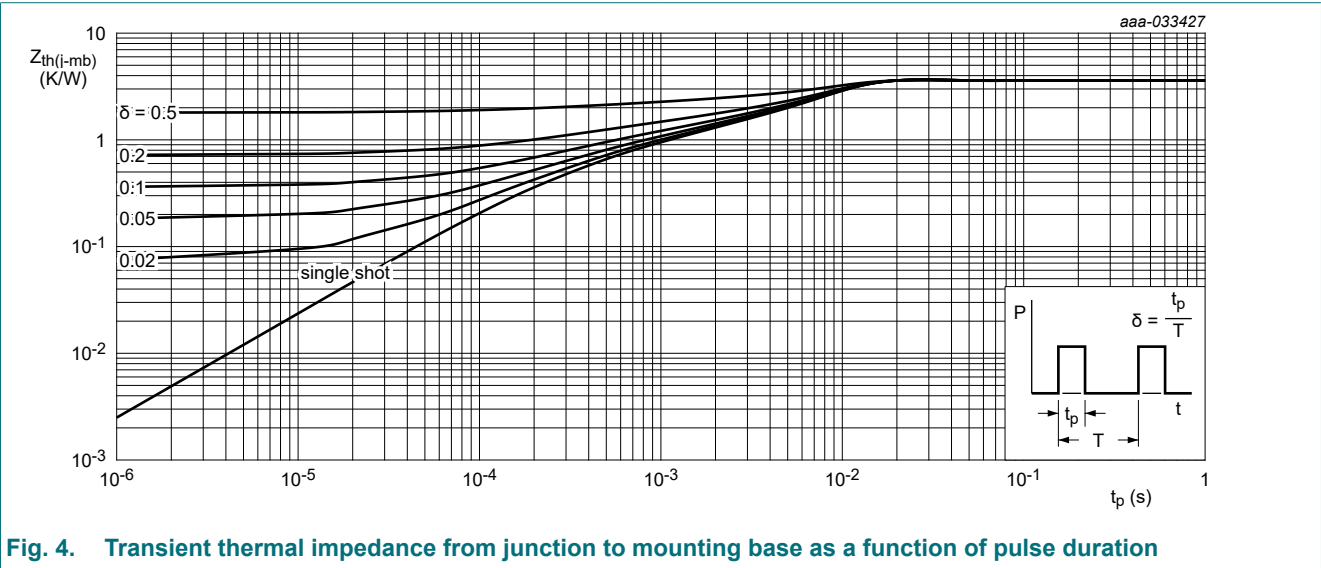
Fig. 2. Continuous drain current as a function of mounting base temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 4	-	3	3.6	K/W



10. Characteristics

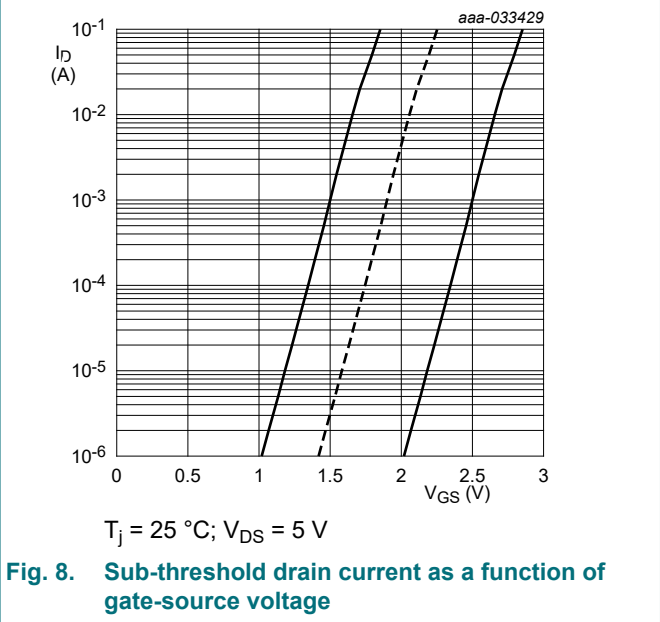
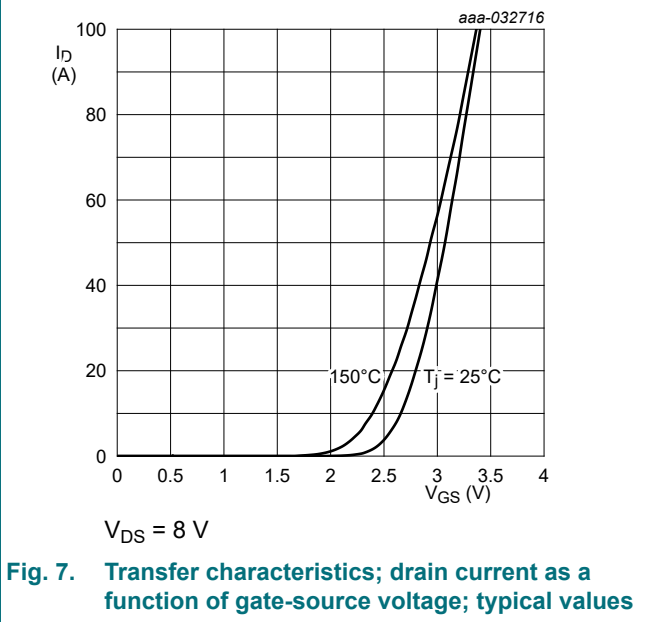
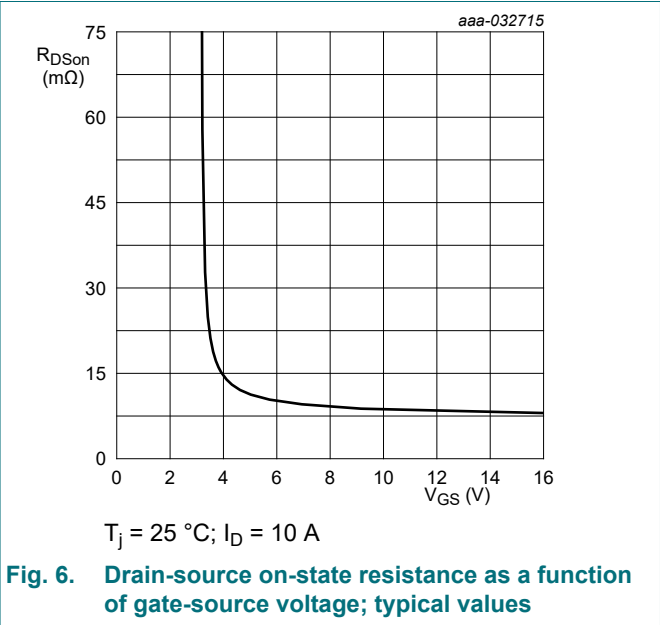
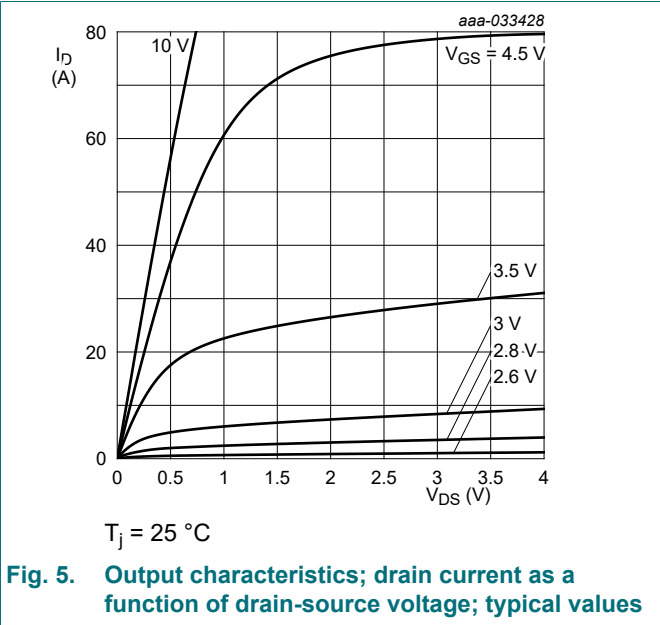
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	60	70	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = -55\ ^\circ C$	-	64	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = 25\ ^\circ C$; Fig. 8	1.5	1.9	2.5	V
		$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = 150\ ^\circ C$	0.9	-	-	V
		$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = -55\ ^\circ C$	-	-	2.9	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\ ^\circ C \leq T_J \leq 150\ ^\circ C$	-	-4.7	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 60\ V$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	-	0.01	1	μA
		$V_{DS} = 60\ V$; $V_{GS} = 0\ V$; $T_J = 150\ ^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	2	100	nA
		$V_{GS} = -20\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 10\ A$; $T_J = 25\ ^\circ C$; Fig. 9	-	9.8	11.5	m Ω
		$V_{GS} = 10\ V$; $I_D = 10\ A$; $T_J = 150\ ^\circ C$; Fig. 10	-	-	20	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 10\ A$; $T_J = 25\ ^\circ C$; Fig. 9	-	14	17.6	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 10\ A$; $T_J = 150\ ^\circ C$; Fig. 10	-	-	30	m Ω
R_G	gate resistance	$f = 1\ MHz$; $T_J = 25\ ^\circ C$	-	1.66	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10\ A$; $V_{DS} = 30\ V$; $V_{GS} = 4.5\ V$; $T_J = 25\ ^\circ C$; Fig. 11 ; Fig. 12	-	9.64	-	nC
		$I_D = 10\ A$; $V_{DS} = 30\ V$; $V_{GS} = 10\ V$; $T_J = 25\ ^\circ C$; Fig. 11 ; Fig. 12	-	18.77	-	nC
		$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 4.5\ V$; $T_J = 25\ ^\circ C$; Fig. 11 ; Fig. 12	-	9.54	-	nC
Q_{GS}	gate-source charge	$I_D = 10\ A$; $V_{DS} = 30\ V$; $V_{GS} = 4.5\ V$; $T_J = 25\ ^\circ C$; Fig. 11 ; Fig. 12	-	3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.6	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.4	-	nC
Q_{GD}	gate-drain charge		-	4.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10\ A$; $V_{DS} = 30\ V$; $T_J = 25\ ^\circ C$; Fig. 11 ; Fig. 12	-	3.1	-	V
C_{iss}	input capacitance	$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_J = 25\ ^\circ C$; Fig. 13	-	957	-	pF
C_{oss}	output capacitance		-	386	-	pF
C_{rss}	reverse transfer capacitance		-	31	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\ V$; $R_L = 3\ \Omega$; $V_{GS} = 4.5\ V$; $R_{G(ext)} = 5\ \Omega$; $T_J = 25\ ^\circ C$	-	8.8	-	ns
t_r	rise time		-	18.5	-	ns
$t_{d(off)}$	turn-off delay time		-	12.2	-	ns
t_f	fall time		-	10.9	-	ns

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$		-	18	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 14		-	0.82	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 15		-	22.1	-	ns
Q_r	recovered charge		[1]	-	13	-	nC

[1] includes capacitive recovery



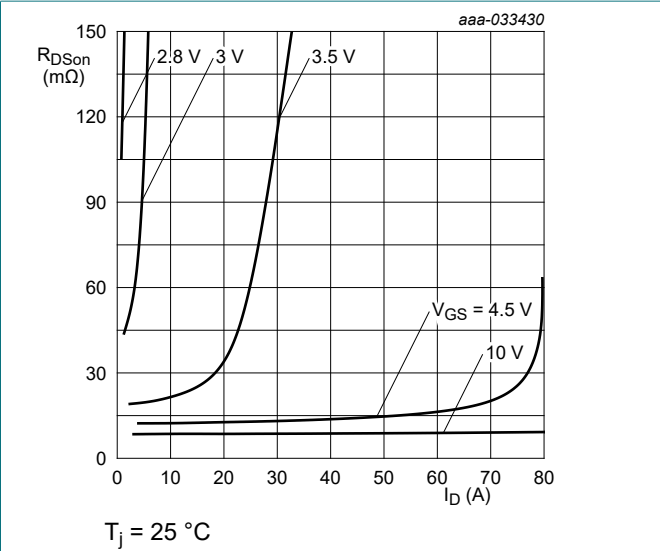


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

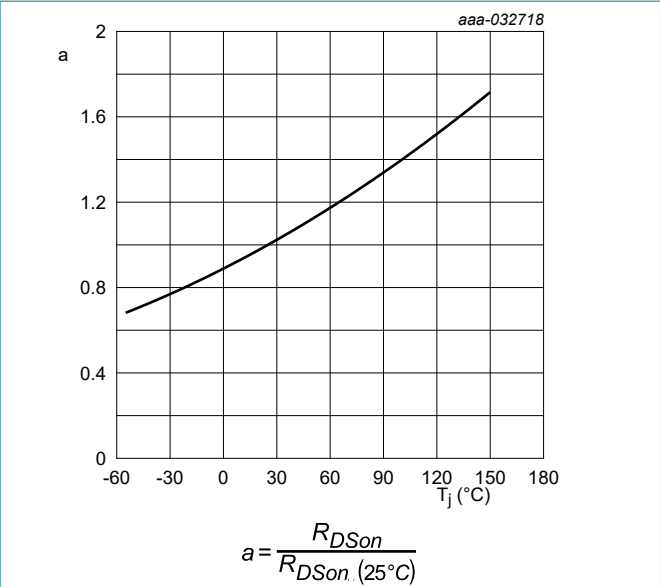


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

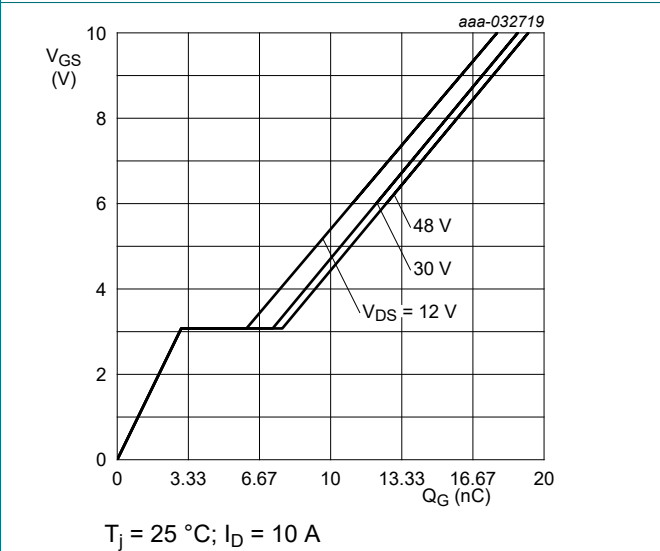


Fig. 11. Gate-source voltage as a function of gate charge; typical values

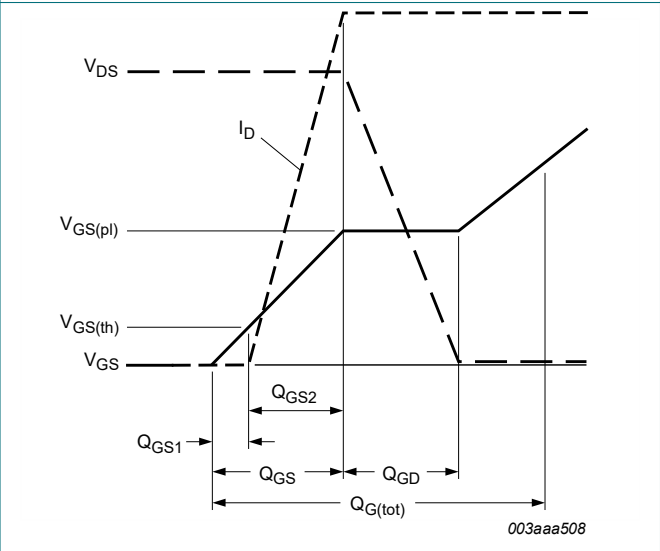


Fig. 12. Gate charge waveform definitions

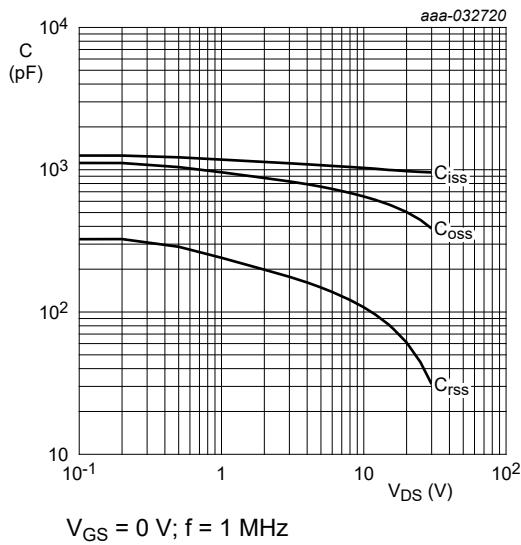


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

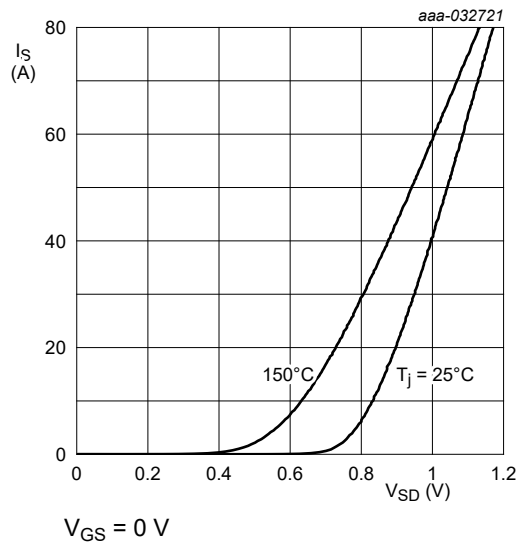


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

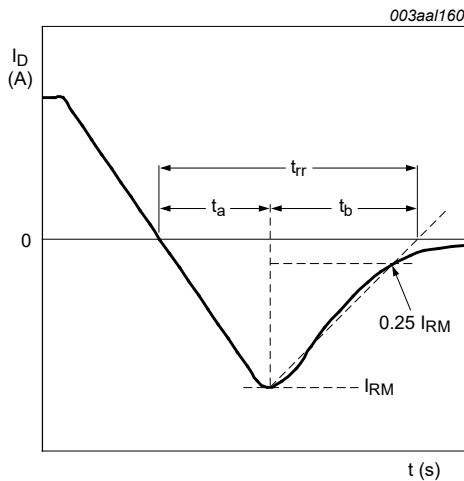


Fig. 15. Reverse recovery timing definition

11. Package outline

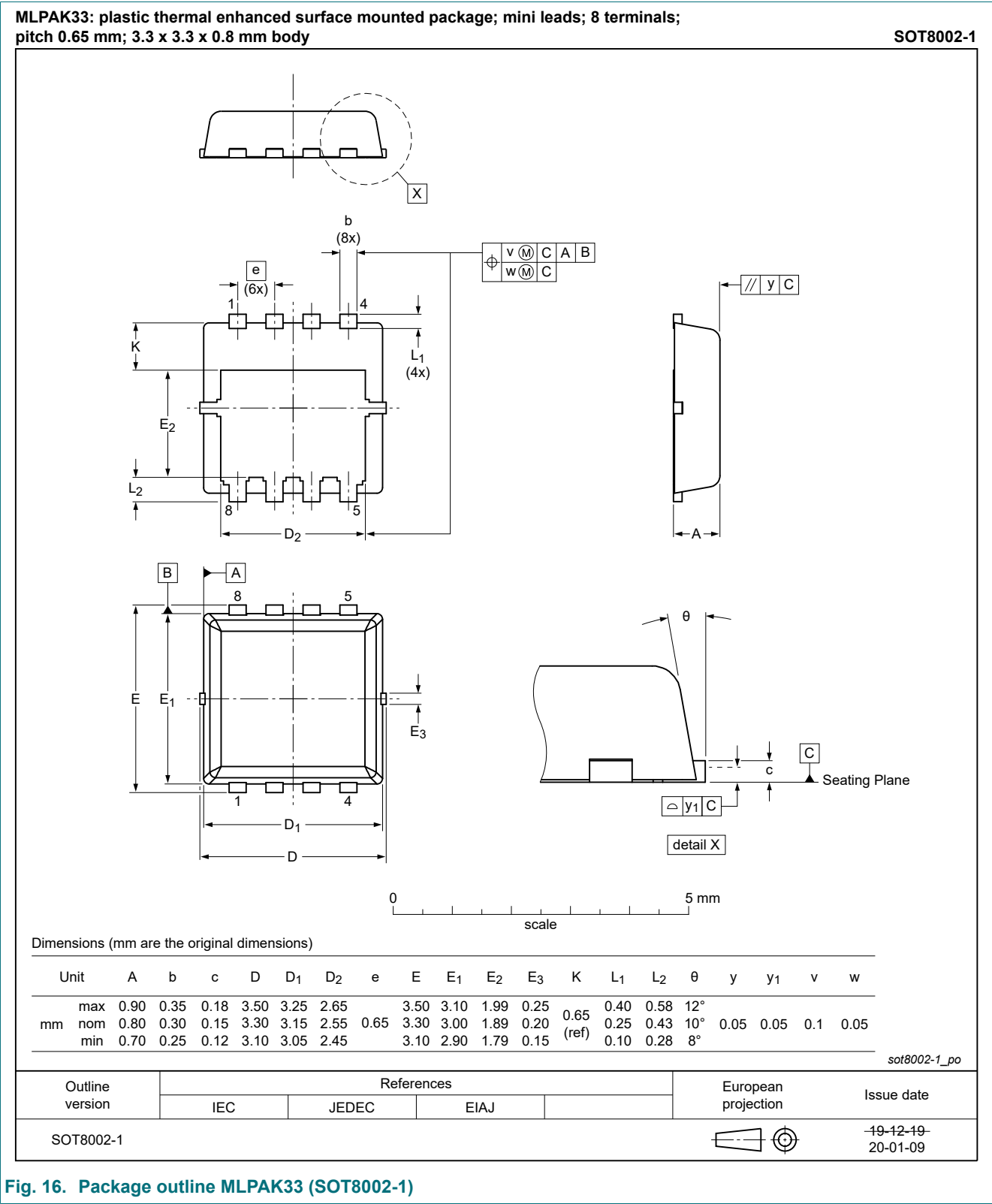


Fig. 16. Package outline MLPAK33 (SOT8002-1)

12. Soldering

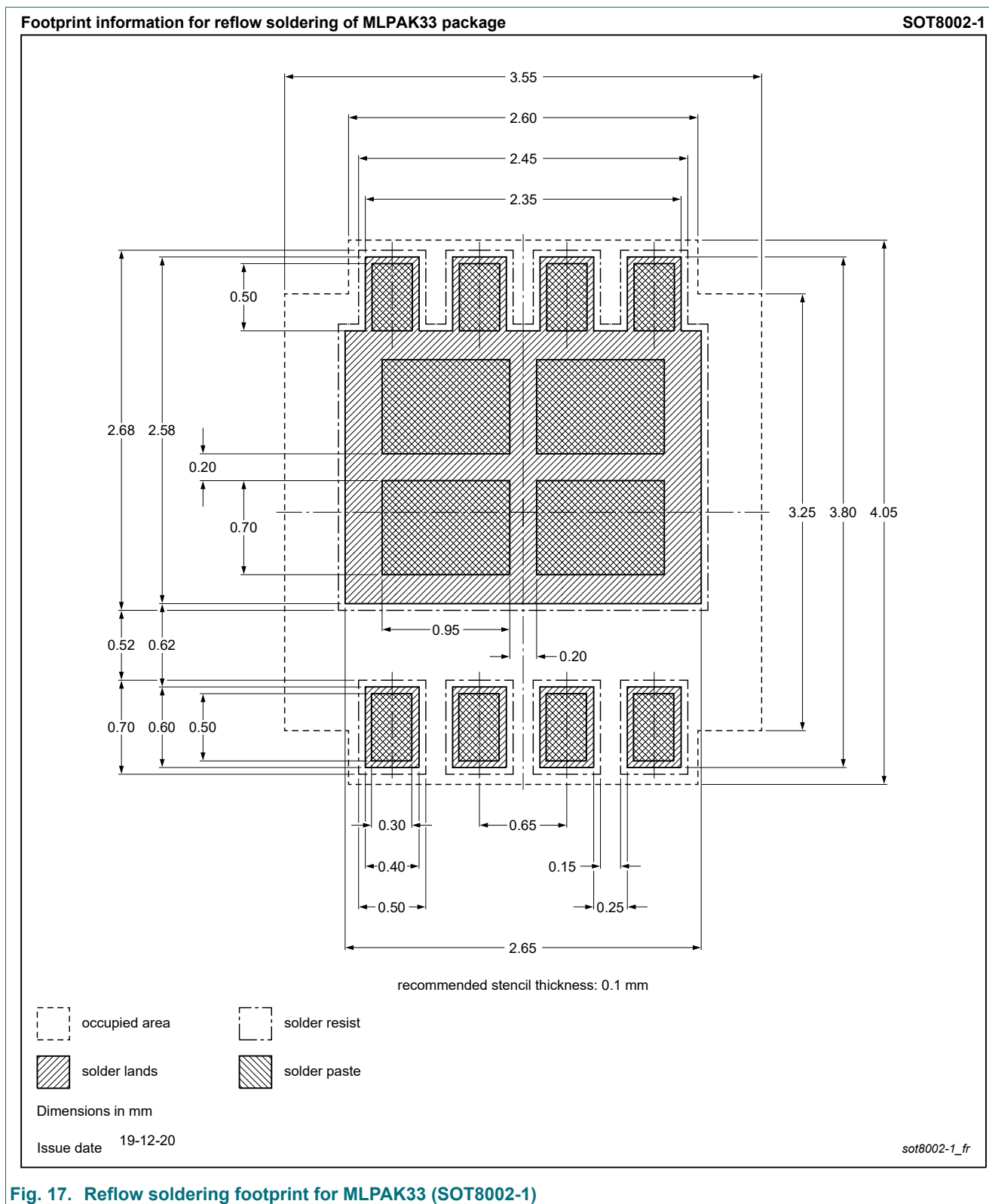


Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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