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MOSFET – Power, Single P-Channel

-40 V, 9.6 mΩ, -71 A

NVTYS9D6P04M8L

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-40	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 4)	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	-71	A
		$T_C = 100^{\circ}\text{C}$		-50	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		$T_C = 25^{\circ}\text{C}$	P_D	75	W
		$T_C = 100^{\circ}\text{C}$		37.5	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	-16	A
		$T_A = 100^{\circ}\text{C}$		-11	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		$T_A = 25^{\circ}\text{C}$	P_D	3.9	W
		$T_A = 100^{\circ}\text{C}$		1.9	
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}, t_p = 10\text{ }\mu\text{s}$		I_{DM}	423	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	62.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain) (Notes 1, 2 and 4)	$R_{\theta JC}$	2	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	38.6	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

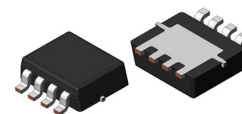
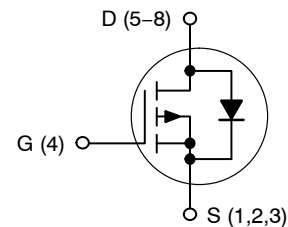


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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-40 V	9.6 mΩ @ -10 V	-71 A
	16 mΩ @ -4.5 V	

P-Channel MOSFET



**LFPAK8
3.3x3.3
CASE 760AD**

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVTYS9D6P04M8L

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	-40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			20		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -40 V			-1.0	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -580 μA	-1	1.65	-3	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -25 A		7.7	9.6	mΩ
		V _{GS} = -4.5 V, I _D = -20 A		11	16	

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -25 V		2368		pF
Output Capacitance	C _{oss}			842		
Reverse Transfer Capacitance	C _{rss}			32		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -10 V, V _{DS} = -20 V, I _D = -25 A		35		nC
Threshold Gate Charge	Q _{G(TH)}			3.1		
Gate-to-Source Charge	Q _{GS}			7.5		
Gate-to-Drain Charge	Q _{GD}			3.9		

SWITCHING CHARACTERISTICS, V_{GS} = -10 V (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -10 V, V _{DS} = -20 V, I _D = -25 A, R _G = 6 Ω		9.6		ns
Rise Time	t _r			29		
Turn-Off Delay Time	t _{d(off)}			187		
Fall Time	t _f			99		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -25 A	T _J = 25°C		-0.88	-1.25	V
			T _J = 175°C		-0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -25 A			45		ns
Charge Time	t _a				21.7		
Discharge Time	t _b				23.3		
Reverse Recovery Charge	Q _{RR}				37	56	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

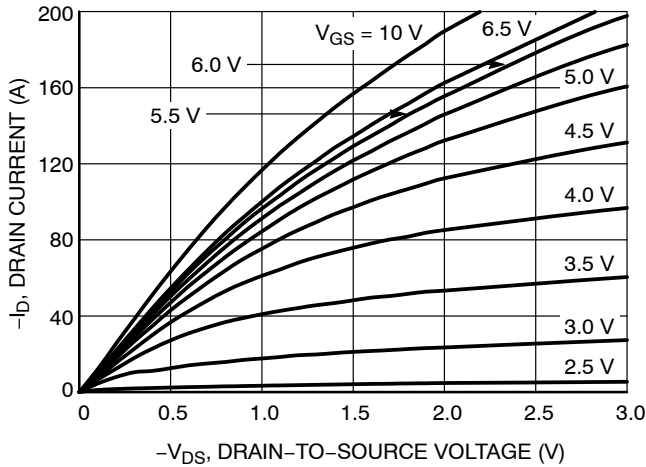


Figure 1. On-Region Characteristics

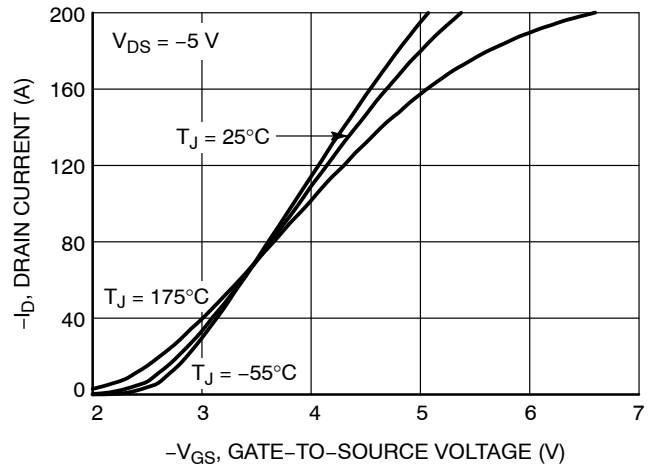


Figure 2. Transfer Characteristics

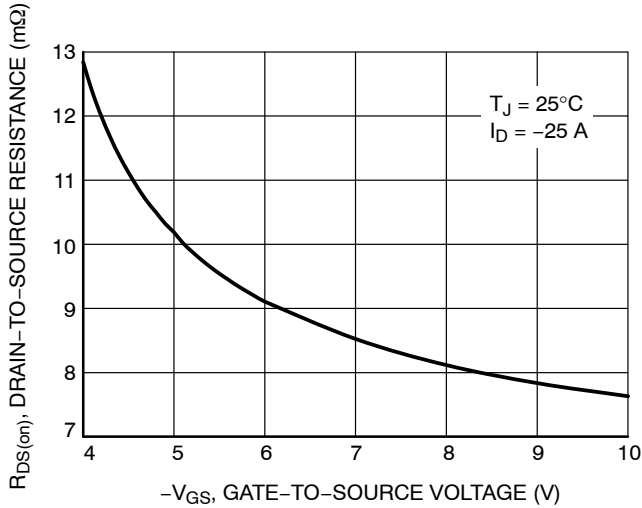


Figure 3. On-Resistance vs. Gate-to-Source Voltage

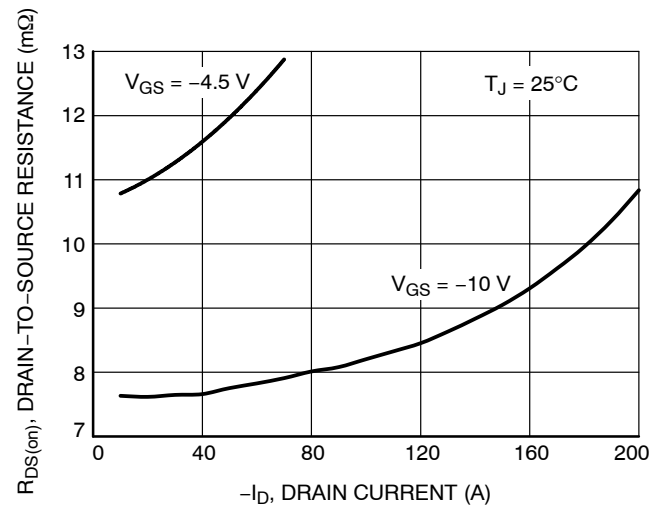


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

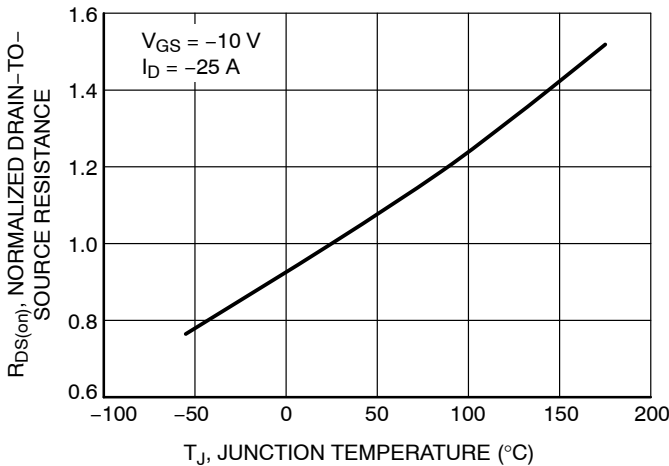


Figure 5. On-Resistance Variation with Temperature

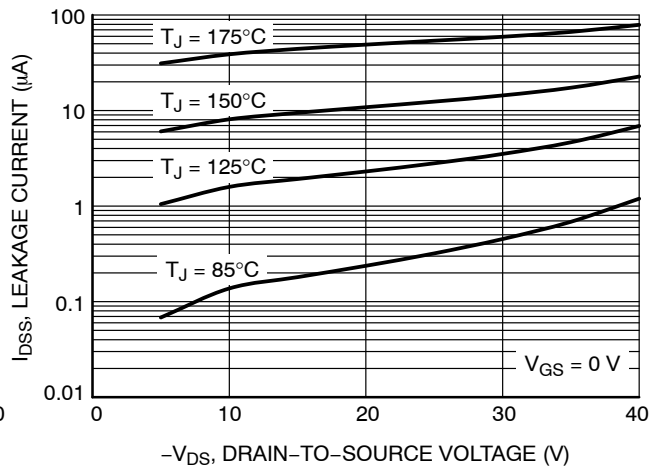


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

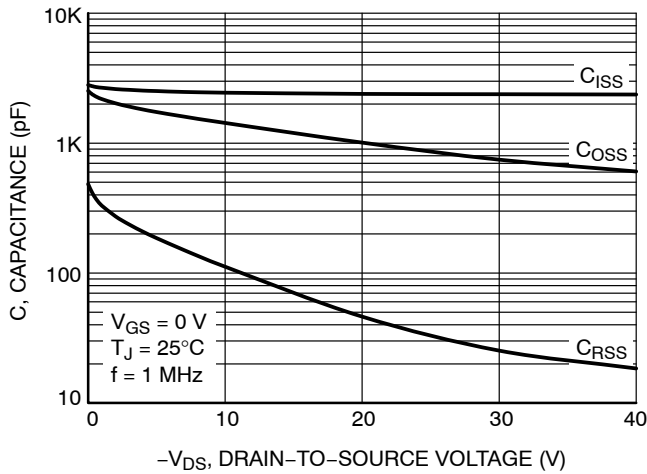


Figure 7. Capacitance Variation

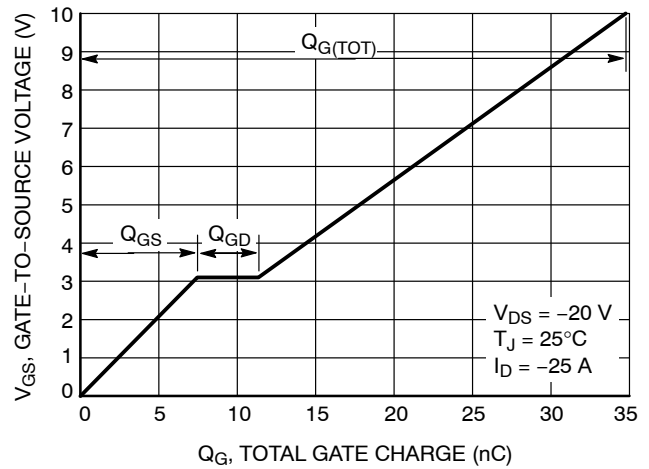


Figure 8. Gate-to-Source Voltage vs. Total Charge

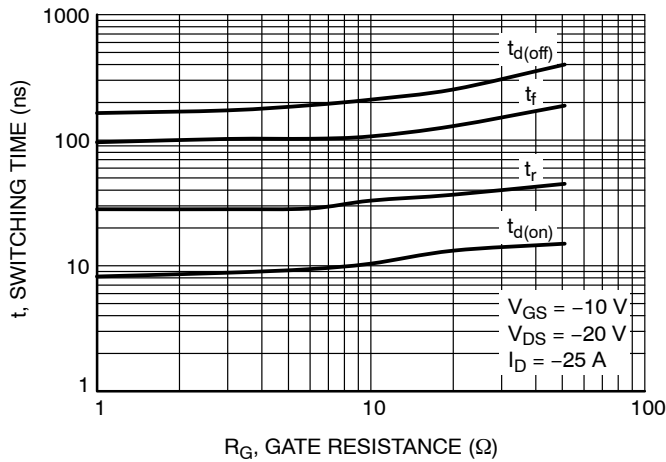


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

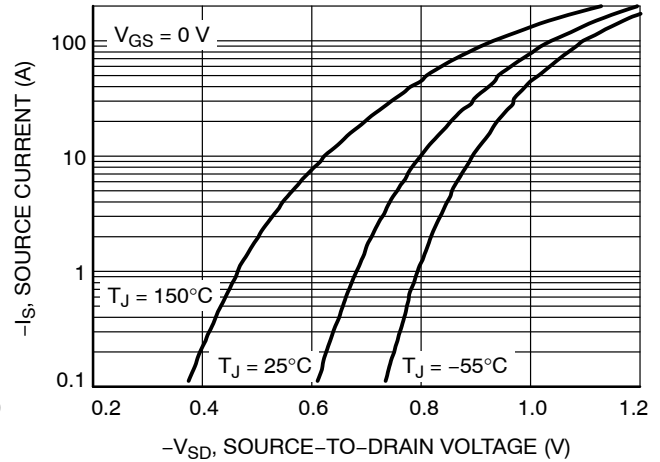


Figure 10. Diode Forward Voltage vs. Current

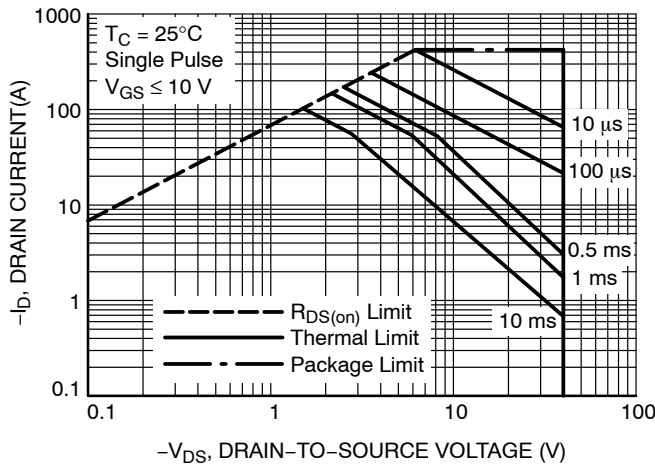


Figure 11. Maximum Rated Forward Biased Safe Operating Area

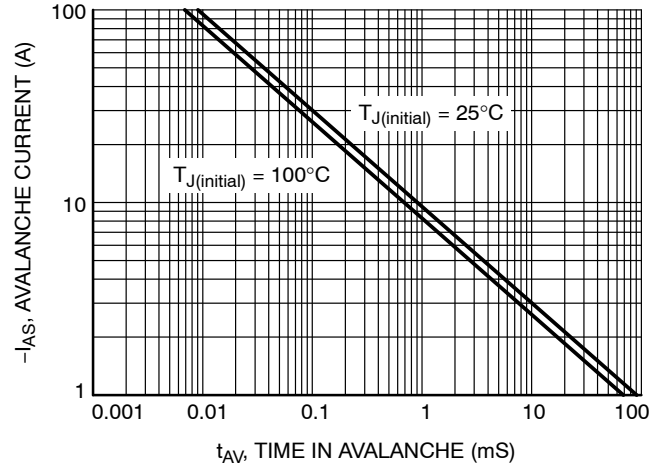


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

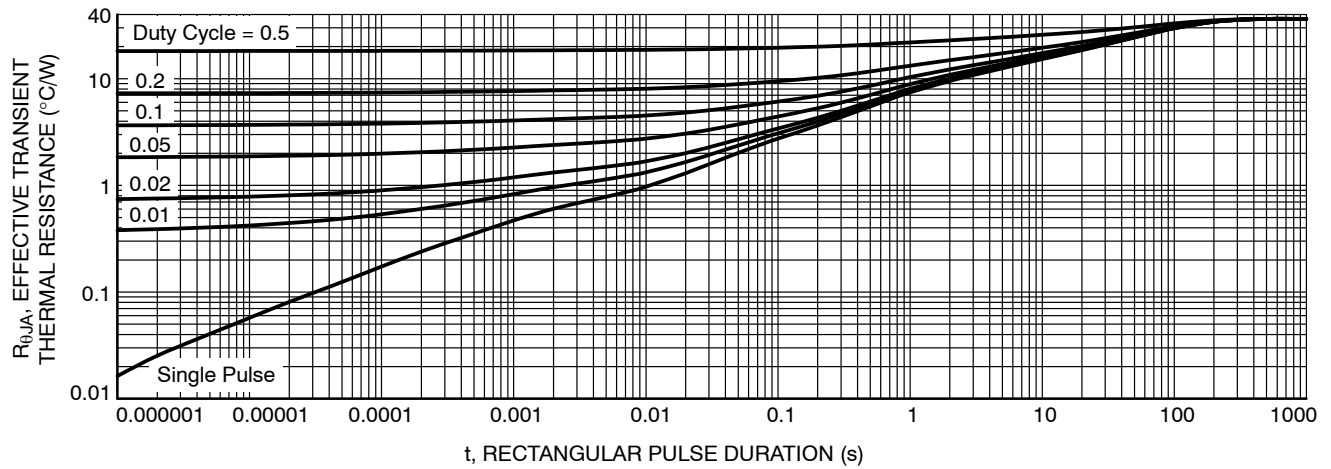


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

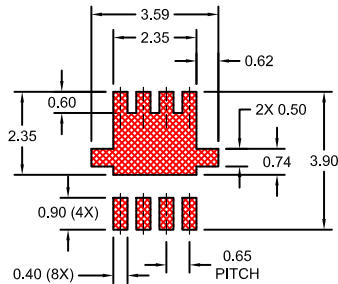
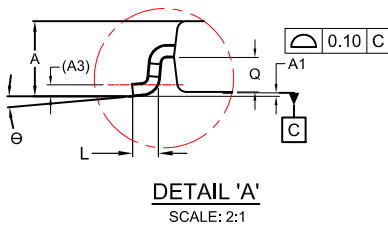
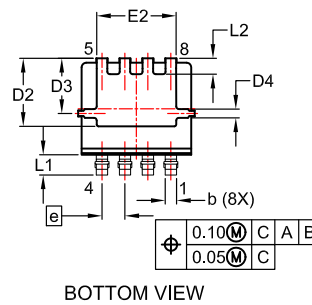
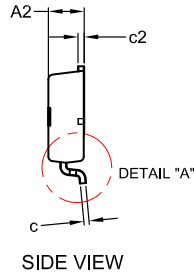
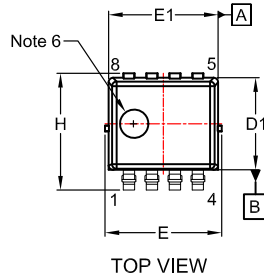
Device	Marking	Package	Shipping [†]
NVTYS9D6P04M8LTWG	9D6P 04M8L	LFPAK33	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVTYS9D6P04M8L

PACKAGE DIMENSIONS

LFPAK8 3.3x3.3, 0.65P CASE 760AD ISSUE E



*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.05	0.10
A2	0.95	1.00	1.05
A3	0.15 REF		
b	0.27	0.32	0.37
c	0.12	0.17	0.22
c2	0.12	0.17	0.22
D1	2.50	2.60	2.70
D2	1.82	1.92	2.02
D3	1.46	1.56	1.66
D4	0.20	0.25	0.30
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	2.15	2.25	2.35
e	0.65 BSC		
H	3.20	3.30	3.40
L	0.25	0.37	0.50
L1	0.48	0.58	0.68
L2	0.35	0.45	0.55
Q	0.45	0.50	0.55
Θ	0°	4°	8°

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