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MOSFET – Power, Single N-Channel, DFNW8 150 V, 6.4 mΩ, 128 A

NVMTS6D0N15MC

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter			Value	Unit
V _{DSS}	Drain-to-Source Voltage			150	V
V _{GS}	Gate-to-Source Voltage			±20	V
I _D	Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 25°C	128	A
P _D	Power Dissipation R _{θJC} (Note 2)			237	W
I _D	Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 100°C	90	A
P _D	Power Dissipation R _{θJC} (Note 2)			119	W
I _D	Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	18	A
P _D	Power Dissipation R _{θJA} (Notes 1, 2)			5	W
I _D	Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 100°C	13	A
P _D	Power Dissipation R _{θJA} (Notes 1, 2)			2.4	W
I _{DM}	Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		900	A
T _J , T _{stg}	Operating Junction and Storage Temperature Range			-55 to 175	°C
I _S	Source Current (Body Diode)			198	A
E _{AS}	Single Pulse Drain-to-Source Avalanche Energy (I _L = 10.2 A _{pk})			2376	mJ
T _L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

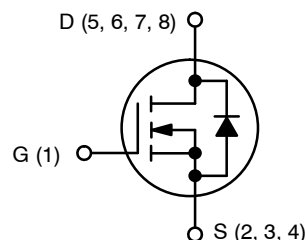
1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted



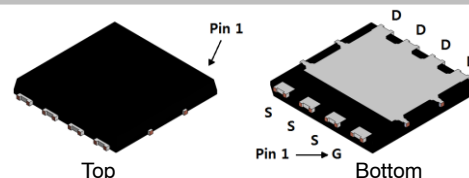
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$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	6.4 mΩ @ 10 V	128 A

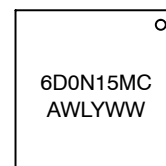


N-CHANNEL MOSFET



DFNW8 8.3x8.4, 2P
PQFN88
CASE 507AP

MARKING DIAGRAM



6D0N15MC = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

Device	Package	Shipping†
NVMTS6D0N15MC	DFNW8 PQFN88 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVMTS6D0N15MC

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 2)	0.63	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	31.6	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA		150	–	–	V
V _{(BR)DSS} / T _J	Drain-to-Source Breakdown Voltage Temperature Coefficient	I _D = 250 μA, ref to 25°C		–	58.67	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 120 V	T _J = 25°C	–	–	1	μA
			T _J = 125°C	–	–	10	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = ±20 V		–	–	±100	nA

ON CHARACTERISTICS (Note 3)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 379\text{ }\mu\text{A}$	2.5	3.6	4.5	V
$V_{GS(TH)} / T_J$	Negative Threshold Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C	–	–9.14	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 69\text{ A}$	–	4.6	6.4	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 69\text{ A}$	–	127	–	S
R_G	Gate-Resistance	$T_A = 25^\circ\text{C}$	–	1.1	–	Ω

CHARGES & CAPACITANCES

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$	–	4815	–	pF
C_{OSS}	Output Capacitance		–	1482	–	
C_{RSS}	Reverse Transfer Capacitance		–	9.7	–	
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 69\text{ A}$	–	58	–	nC
$Q_{G(TH)}$	Threshold Gate Charge		–	34	–	
Q_{GS}	Gate-to-Source Charge		–	26	–	
Q_{GD}	Gate-to-Drain Charge		–	8	–	
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$	–	173	–	nC

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 69\text{ A}, R_G = 6\text{ }\Omega$	–	30	–	ns
t_r	Rise Time		–	7	–	
$t_{d(OFF)}$	Turn-Off Delay Time		–	38	–	
t_f	Fall Time		–	6	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 69 A	T _J = 25°C	–	0.87	1.2	V
			T _J = 125°C	–	0.70	–	
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 69 A		–	72	–	ns
t _a	Charge Time			–	49	–	
t _b	Discharge Time			–	23	–	
Q _{RR}	Reverse Recovery Charge			–	125	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

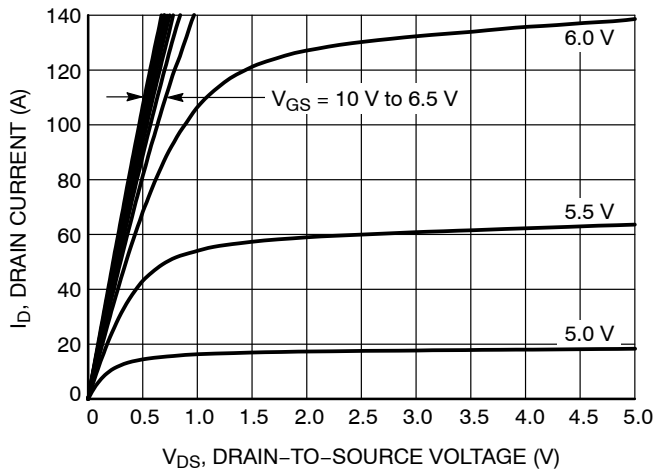


Figure 1. On-Region Characteristics

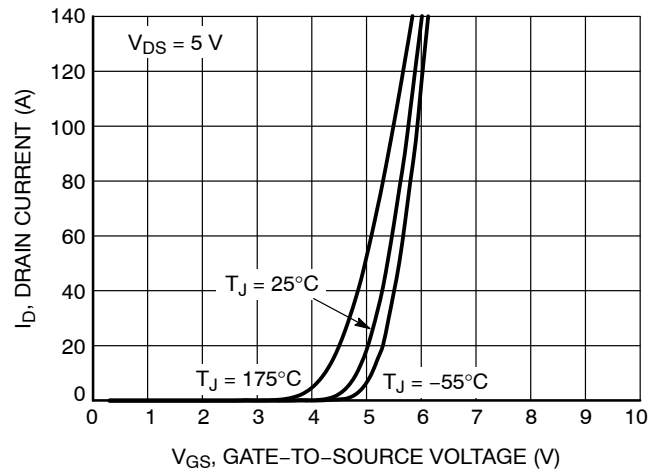


Figure 2. Transfer Characteristics

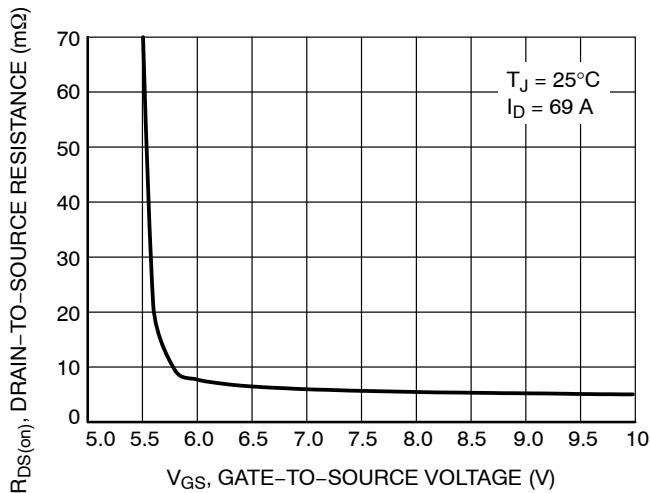


Figure 3. On-Resistance vs. Gate-to-Source Voltage

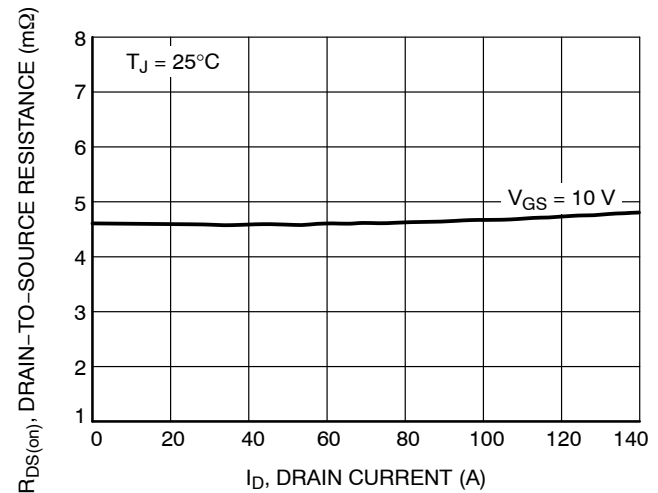


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

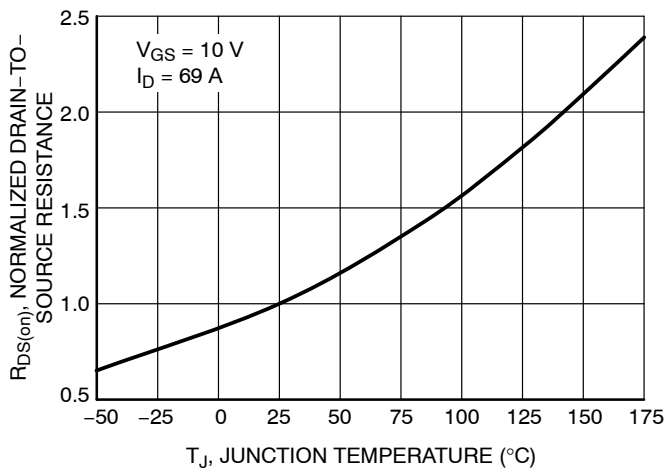


Figure 5. On-Resistance Variation with Temperature

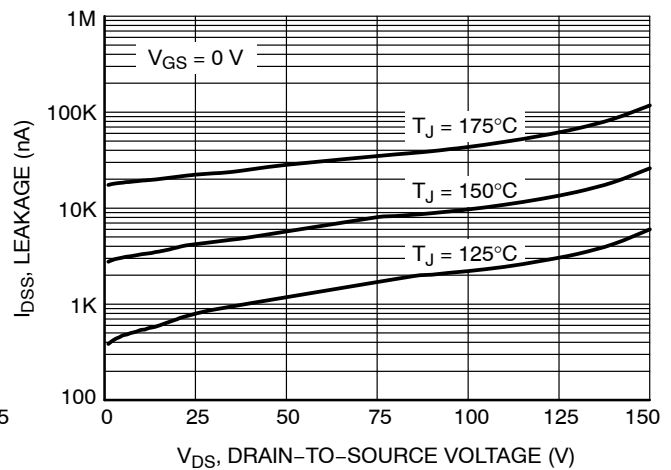


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

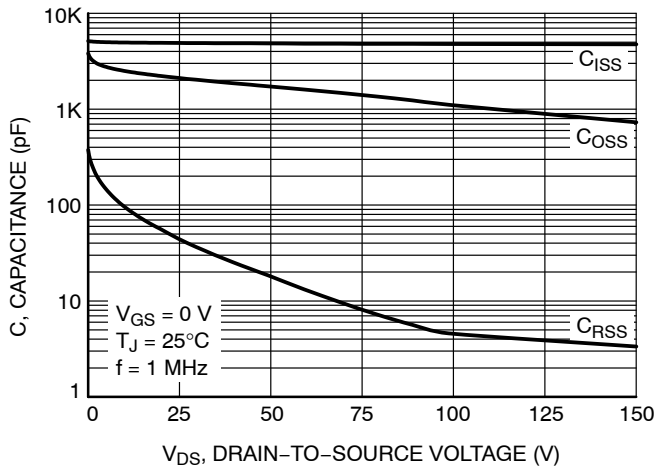


Figure 7. Capacitance Variation

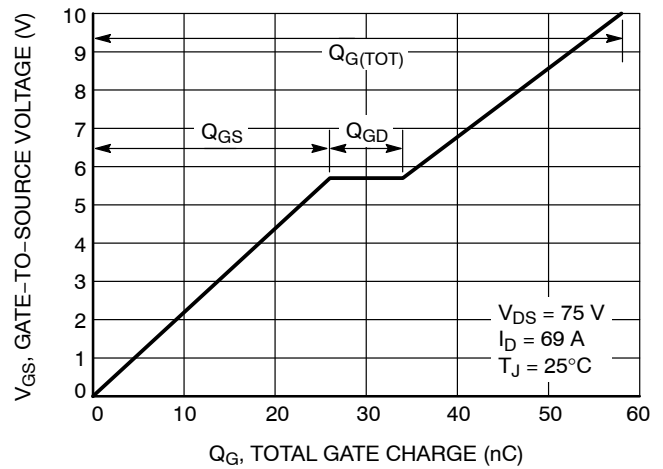


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

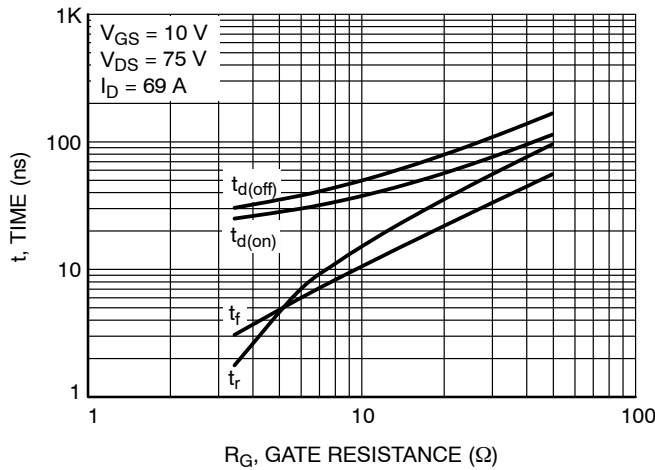


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

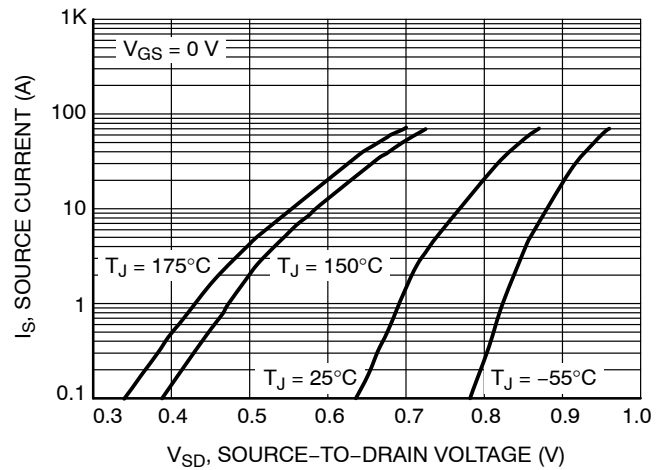


Figure 10. Diode Forward Voltage vs. Current

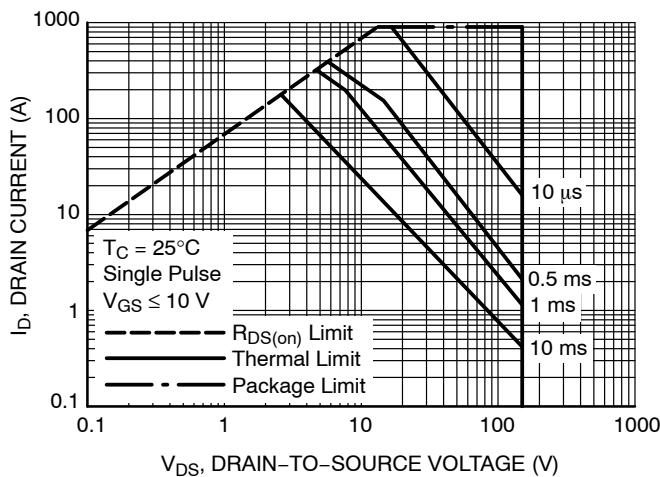


Figure 11. Safe Operating Area

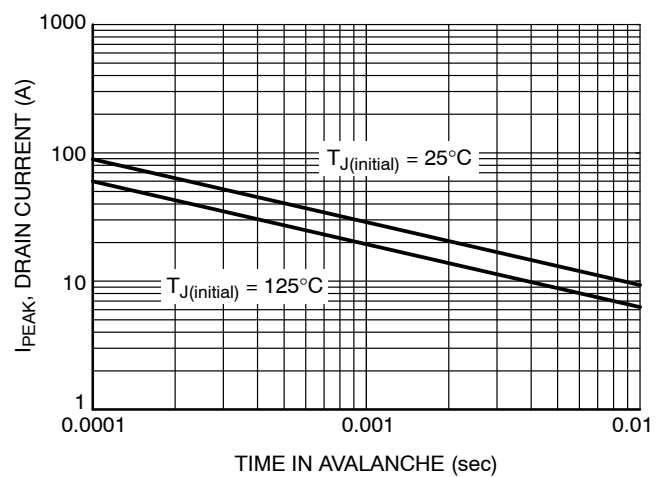


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

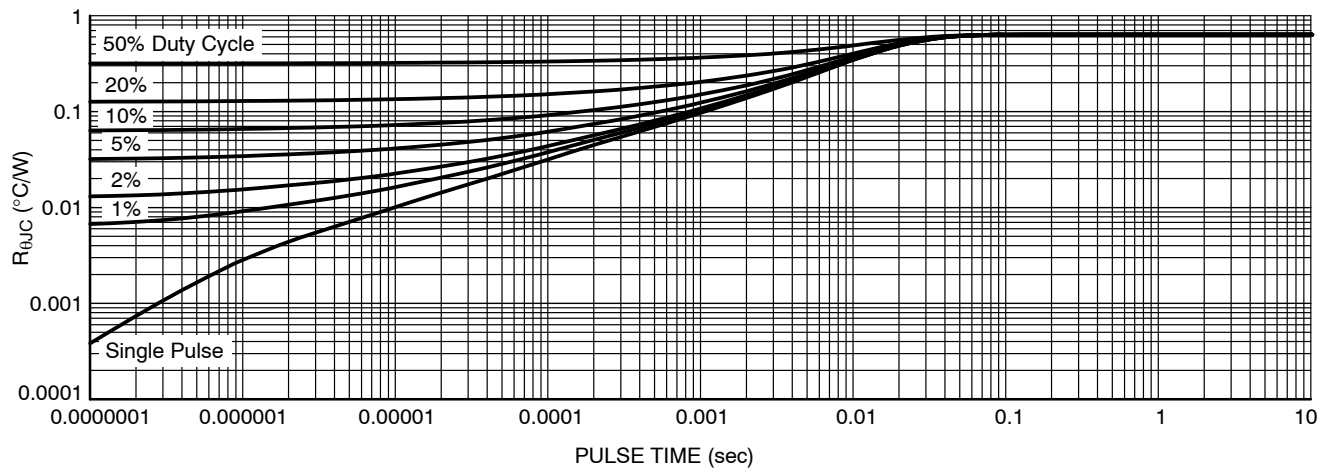


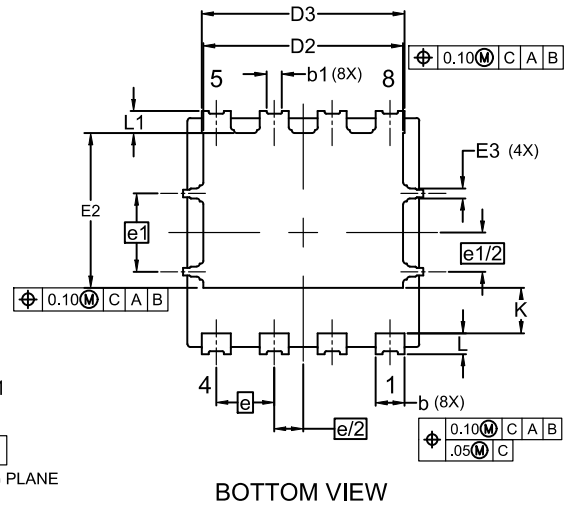
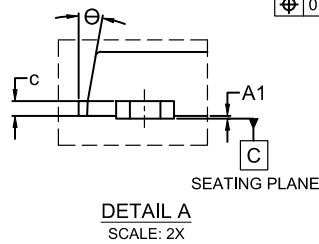
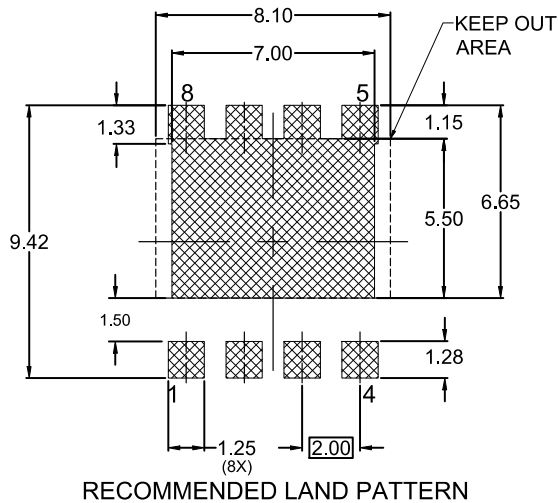
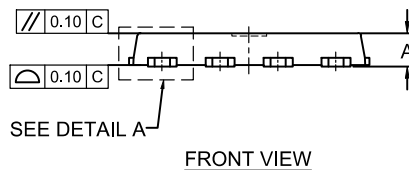
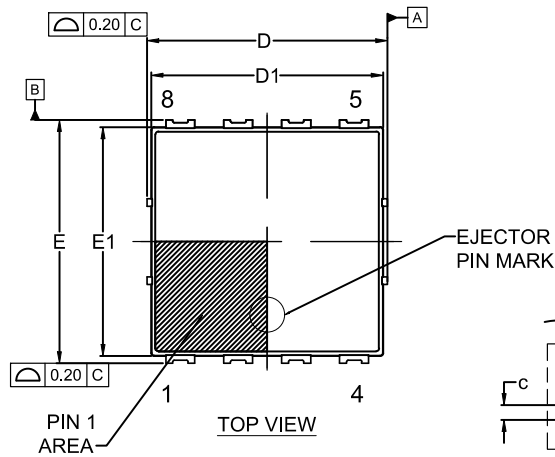
Figure 13. Thermal Characteristics

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PACKAGE DIMENSIONS

DFNW8 8.3x8.4, 2P
CASE 507AP
ISSUE A

DATE 14 AUG 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS.
"A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	---	0.05
b	0.90	1.00	1.10
b1	0.43	0.53	0.63
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	---	12°

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